Systematic Design for Optimization of High-Resolution Pipelined ADCs

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ABSTRACT

Pipelining is the promising approach to implement high-speed medium-to-high resolution analog-to-digital converters with minimum power consumption. In this paper, the most important specifications of a pipelined ADC including the signal-to-noise-and-distortion ratio and spurious-free dynamic range as well as the total current consumption of the converter are presented in closed-form equations and an optimization methodology for design of pipelined ADCs is suggested. Simulation results confirming the effectiveness of the methodology are presented.

1. Introduction

Design approaches to reduce the power consumption of pipelined ADCs are of great importance to realize medium-to-high-resolution high-speed A/D converters with the least possible power consumption [1-3]. In this abstract, an optimized design methodology for high-resolution pipelined ADCs based on closed-form formulas previously reported by the authors [1-2] is described. The contribution of this abstract compared to the previous papers [1-3] is in relating the SFDR and SNDR values to the absolute values of the capacitors. Therefore, employing the previously developed equations for the total power consumption and the total input-referred thermal noise, the optimization criteria are completed now.

In this brief, after a short review on the way the previously reported parameters are extracted, the values of the SFDR and SNDR are related to the absolute values of the capacitors by employing the mismatch-variance vs. absolute-value curve of the capacitors. All important dynamic non-linearity and noise parameters are now fully analyzed in order to optimize the converter for minimum power dissipation. Design examples are included to illustrate the capabilities of the methodology.

2. Calculation of the Current Consumption

Employing an optimized procedure to dynamically determine the contributions of the slewing and settling behaviors in the total settling time for an operational amplifier in a switched-capacitor circuit, the optimized value of the current consumption of an individual opamp has been expressed versus the values of the sampling frequency, the full-scale voltage, the feedback factor and the load capacitors [1]. Expressing the load capacitance and also the feedback factor of the opamp in a residue amplifier as functions of the capacitors and the resolutions of the residue stage and those of the following stage, the total current consumption of the OTAs are calculated. Considering the current consumption of the comparators, the total current consumption of the ADC is therefore obtained [1].

3. SFDR Calculation

In order to determine the SFDR in an ADC, the harmonic component of each stage should be calculated. It can be seen that the biggest harmonic component of each stage is the third one [2]. The third harmonic of the stages should be referred to the input by dividing by gains of the previous stages and summing them accordingly to determine the total third harmonic of the converter. As presented in [2] the input-referred third harmonic component of the converter has a normal distribution with the variance value of

$$\left(\sigma^2_{a_3}\right)_i = 0.155^2 \cdot 2^{2\left(1-\sum_{j=1}^{i} m_j\right)}\left(\sigma^2_{\delta g_i} + \left(2^{m_i}-1\right)\sigma^2_{\delta C_i} - \frac{1}{2^{2m_{i+1}}}\sigma^2_{\delta C_{i+1}}\right) \quad (1)$$

where $\sigma^2\delta g_i$ and $\sigma^2\delta C_i$ are the variances of the random variables of the capacitance mismatch and the gain error of the *i*th residue stage respectively. m_i is the effective resolution of the *i*th stage.

In order to calculate the spurious-free dynamic range of the pipelined ADC, the largest harmonic component should be determined. It is known that the largest harmonic component (H_q) caused by the quantization non-linearity is $9N$-c dB below the fundamental component where N is the ADC resolution and c is varied between 0 and 8 depending on the converter resolution [4]. Therefore, it can be concluded that the magnitude of the largest spurious signal is the maximum value of either a_3 or H_q. As a result, the SFDR is obtained from

$$SFDR = \min\left\{9N - c, 20\cdot\log(1/a_3)\right\} \quad (2)$$

As mentioned before, a_3 is a random variable where its variance value was derived in (1). In order to estimate the one-sigma SFDR, one can start of one-sigma a_3 represented by σ_{a_3}. So we have [2]

$$SFDR = \min\left\{9N - c, 16.2 - 10\cdot\log(\Delta E)\right\} \quad (3)$$

where

$$\Delta E = \sum_{i=1}^{n} 2^{2\left(1-\sum_{j=1}^{i} m_j\right)}\left(\left(2^{m_i}-1\right)\sigma^2_{\delta C_i} + \sigma^2_{\delta g_i} - \frac{1}{2^{2m_{i+1}}}\sigma^2_{\delta C_{i+1}}\right) \quad (4)$$

4. SNDR Calculation

The total input-referred spurious power of the converter is obtained from

$$P_{spur} = \sum_{i=2}^{\infty}\left(a_i/\sqrt{2}\right)^2 \quad (5)$$

where a_i is the magnitude of the *i*th input-referred harmonic component of the entire converter and the fundamental component signal has the magnitude of a_1. Assuming no correlation between the harmonic components of the ADC stages, this distortion plus noise power has been calculated as [2]

$$P_{spur} = P_{dstr} + {V_{FS}}^2/\left(12\times 2^{2n}\right) + P_{n,th} \quad (6)$$

where the distortion power of the ADC, P_{dstr} is obtained from [2]

$$P_{dstr} = \frac{V_{FS}^2}{50}\left(\sum_{i=1}^{N}(1.9)^{2\left(1-\sum_{j=1}^{i} m_j\right)}\left(\left(2^{m_i}-1\right)\sigma^2_{\delta C_i} + \sigma^2_{\delta g_i} + \frac{1}{2^{2m_{i+1}}}\sigma^2_{\delta C_{i+1}}\right)\right) \quad (7)$$

where V_{FS} is the full scale voltage of the ADC. The second term in (6) represents the distortion caused by the quantization non-linearity and the third term is the total input-referred thermal noise of the converter. Having known $P_{signal}=V^2_{FS}/8$, the total SNDR is obtained as

$$SNDR = 6.02n - 10\log\left(2^{2n+1}\left(P_{dstr} + P_{n,th}/\left(V_{FS}^2/4\right)\right) + 0.667\right) \quad (8)$$

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where the total input-referred noise power of the *n*-stage pipelined ADC is obtained from [1]

$$P_{n,th} = kT \sum_{j=1}^{n} \left(\frac{4}{3} \frac{F}{C_{load,j}} + \frac{2}{C_{F,j}} \right) \left(2^{-m,j} + \gamma_j 2^{-2m,j} \right) \Big/ \left(2^{\,2\sum_{i=1}^{j-1} m_i} \right) \quad (9)$$

where undefined parameters were described in [1].

5. Design Methodology

So far the most important specifications of the ADC including the SNR, SNDR, and SFDR and also the total current consumption [1] have been expressed versus the capacitors and the resolutions of the stages. The matching parameter, $\sigma_{\delta C}$ is assumed proportional to $1/C^{½}$ with a proportionality factor extracted from process models. The minimum matching error has been assumed larger than 0.05%.

In this section a systematic design methodology for the resolutions and the capacitor values of a pipelined ADC is proposed by which the design targets of SNR, SNDR and SFDR are satisfied while the power consumption is minimized. Based on the application, the pipelined ADC is optimized for SNR and/or SFDR specification. For example, in imaging applications the SNR is more important than SFDR whereas for software radios SFDR is of more importance.

5.1. SNR- and SNDR-based optimization

Using MATLAB, a simple optimization tool has been developed that employs the proposed closed-form formulas of total current and input-referred noise of the ADC. The optimization problem is defined as follows.

Find the optimum values of the capacitors and the resolutions of stages, in order to minimize the total power consumption of the ADC, while the total input-referred noise requirement is satisfied.

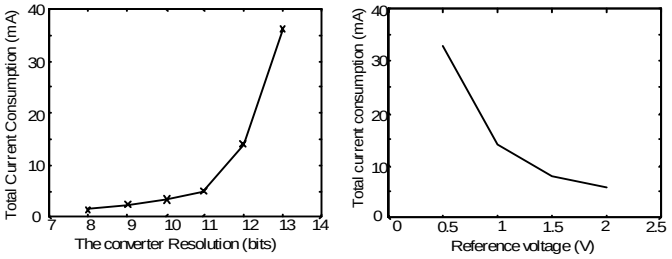
The main parameters of the sub-blocks of the converter including the capacitor values and the resolutions of different stages are *simultaneously* determined in order to minimize the power consumption while no limiting assumption is imposed. The optimization tool is very fast and accurate since the employed equations include all the non-ideal effects. Since the values of γ, ε and F were just the initial estimations, a few iterations accompanied with circuit simulations are required to modify the optimized values of the parameters.

Fig. 1-a shows the optimized current consumption of a 50MS/s converter versus its resolution. The dependency of the power dissipation on the full-scale voltage can also be investigated as shown in Fig. 1-b for a 12-bit 50MS/s ADC. It can be seen that if the full-scale voltage is halved, the current consumption is increased by a factor more than two. Therefore the *power* consumption of the ADC increases by scaling down the voltage.

Fig. 2 shows the required value for the first stage unit capacitor (2-a) and also the optimized value of the total current consumption (2-b) of a 12-bit 50-MSps ADC for different values of SNDR. The plots confirm that the proposed CAD tool can help the designer to optimally design for a specific SNDR.

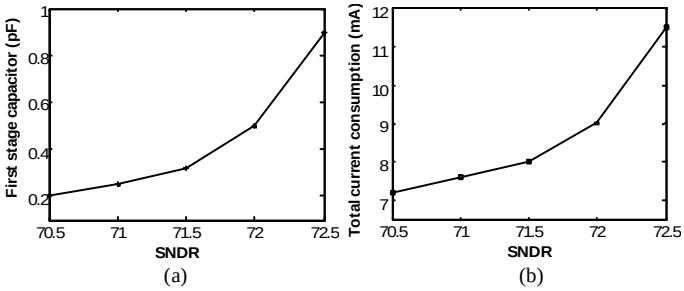
5.2. SFDR-based optimization

Similarly, for an SFDR-based optimization, our proposed formulas have been employed. Then the optimum values of the capacitors and the resolutions of the stages are determined. Fig. 3 shows the required value for the feedback capacitor of the first stage of a 14-bit pipelined ADC with a fully-differential reference voltage of $2V_{p\text{-}p}$ for different values of SFDR. The optimum values for the effective stage resolutions are obtained as [4,1,…1]. It is observed that to increase the SFDR value by 3dB the capacitor values is almost doubled.



(a) (b)

Figure 1. The optimized current consumption of the 50MS/s converter versus (a) its resolution for a full-scale voltage swing of 1V, (b) its full-scale voltage swing for a resolution of 12 bits.



(a) (b)

Figure 2. The required value for (a) the first stage unit capacitor (b) current consumption of the converter to meet a specific SNDR for a 12- bit 50MSps converter.

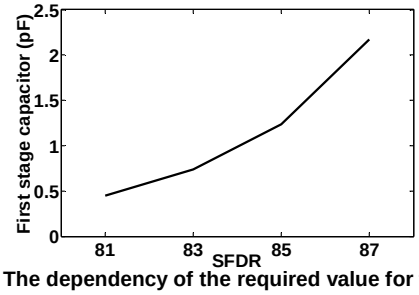


Figure 3. The dependency of the required value for the unit cap. of the first stage on the goal value of the SFDR for a 14-bit ADC.

6. Conclusion

An optimized systematic design methodology has been presented, suggesting the optimum values for the resolutions and the capacitors of all the stages in a pipelined ADC. Employing closed-form formulas for the SNR, SNDR, SFDR and the total current consumption, the optimum values of the capacitors and the resolutions of all stages are simultaneously determined in order to minimize the power consumption while the other specifications are satisfied.

7. References

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