A Methodology for System-Level Analog Design Space Exploration

F. De Bernardinis[†§] and A. Sangiovanni Vincentelli[†]
{fdb, alberto}@eecs.berkeley.edu
[†]Department of EECS, University of California, Berkeley
[§]Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Italy

ABSTRACT

This paper describes a novel approach to system level analog design. A new abstraction level –the platform– is introduced to separate circuit design from design space exploration. An Analog Platform encapsulates analog components concurrently modeling their behavior and their achievable performances. Performance models are obtained through statistical sampling of circuit configurations. The design configurations space is specified with Analog Constraint Graphs so that the sampling space is significantly reduced. System level exploration can be achieved through optimization on behavioral models constrained by performance models. Finally, an example is provided showing the effectiveness of the approach on a WCDMA amplifier.

1. INTRODUCTION

In order to cope with the increasing complexity of modern systems, the concept of platform has been introduced to facilitate design exploration, IP reuse and integration of complex systems [1]. We are firmly convinced that the platform paradigm [2] should be pushed down to the analog level. An *Analog Platform* (AP) is a pre-characterized library of components that can be used to implement analog functionalities. The main purpose of introducing APs is to generate a *new abstraction level* in analog design, so that an effective decoupling is achieved between system level (analog) design and circuit design and synthesis.

The design process starts with the collection/generation of a suitable platform library for system implementation. The platform concept is extremely flexible in terms encapsulation of design components. For example, schematics coming from previous designs, module generators, analog IPs and eventually new solutions can be used to generate a platform library. The result of the exploration phase is a set of specifications for each platform in the system. The exploration process can then be iterated over single sub-systems. Eventually, the evaluation scheme used to estimate platform performances (e.g. simulation) can be inverted so that specifications get converted in suitable configuration parameters. This set of potential solutions could then be used as initial points of a local detailed optimization process, such as finalizing circuit sizing and layout.

2. ANALOG PLATFORMS

An analog platform consists of performance models $\mathcal{P}(\zeta)$ and of behavioral models $\mu(in, out, \zeta)$. $\mu(in, out, \zeta)$ is parameterized executable model that introduces at the functional level a number of non-idealities due to the actual circuit implementation. ζ is a vector of parameters controlling the actual behavior of the model. $\mathcal{P}(\cdot)$ is a relation on ζ. In order to encapsulate and hide all the details of the implementation, non-idealities are modeled in terms of the effects they introduce (e.g. distortion) rather than in term of their causes (transistor sizes or particular topologies). Even if behavioral models introduce non idealities in the block behavior, they are still *functional* models without quantitatively defined architectural effects that arise when the analog functionality (e.g. amplification) is mapped onto an architecture (a specific topology of amplifier).

Analog Platforms can be generated at multiple levels of abstraction. Platforms can be hierarchically organized into platforms stacks. At each level of the stack, an optimization process based on proper platform-dependent methods allows mapping constraints from one level to the next. Platform stacks provide a unifying framework to model both the system abstraction hierarchy and the system refinement process. A key issue with platform stacks is performance models constrain behavioral optimizations/explorations to the feasibility region of the current platform level, so that the next level constraints be feasible and exploration can proceed. Therefore, top-down methodologies can be effectively supported by platform-based design flows.

Performance models constrain behavioral models to behave consistently with the implementation architecture, introducing relations among behavioral model parameters that have to hold for the behavior to be consistent. Because of the nature of analog designs, performance models have to characterize continuous variations in performance as a function of continuous variation of design parameters. Performance parameters for APs are derived bottom-up from simulation data. Differently from common approaches based on simulations that rely on regression schemes, such as [3], relations on performance parameters are directly modeled by means of characteristic functions [4]. Hiding architecture parameters (regression variables) allows design flows to actually proceed top-down and enables different architectures to be directly compared based on the effects they introduce. Given a behav-

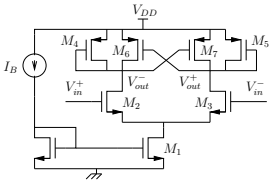

Figure 1: Schematic of the single g_m/g_m stage.

1530-1591/04 $20.00 (c) 2004 IEEE

Stage	$(W \cdot L)_{in}$	*gain*	*noise*	*BW*	*power*	$(W \cdot L)_{out}$	ϵ'_{ave}	$\epsilon'_{\max}$	ϵ''_{ave}	$\epsilon''_{\max}$
1	$0.8 \cdot 10^{-13}$	5.9	$4.1mV$	$4.9GHz$	$52\mu W$	$3.6 \cdot 10^{-13}$	1.37%	2.88%	2.0%	4.3%
2	$3.6 \cdot 10^{-13}$	1.6	$1.3mV$	$5.4GHz$	$52\mu W$	$4.3 \cdot 10^{-13}$	1.5%	3.8%	1.9%	5.3%
3	$4.3 \cdot 10^{-13}$	2.9	$1.9mV$	$6.1GHz$	$54\mu W$	$9.9 \cdot 10^{-13}$	2.8%	5.1%	2.2%	6.6%

Table 1: Optimization results for the amplifier with 3 stages. For each amplifier stage, the basic performance figures are reported and for each performance variable ζ_i the maximum and average relative error $\epsilon = |\zeta_i - \bar{\zeta}_i|/range(\zeta_i)$ is reported for the two closest simulated designs $\bar{\zeta}$.

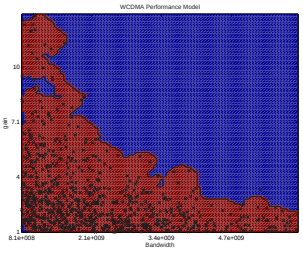

Figure 2: 2D projection of $\mathcal{P}$ on the Gain-Bandwidth plane. The red area is the feasible region. Simulation data are superimposed with crosses.

ioral model $\mu(in, out, \zeta)$, a performance model $\mathcal{P}$ constrains μ to feasible values of ζ ($\mathcal{P}(\zeta) = 1$). Performance models are defined by *Input space* $\mathcal{I}$, *Output space* $\mathcal{O}$, *Evaluation function* ϕ and the *Performance relation*.

The parameter space $\mathcal{I}$ of a circuit is usually much smaller than its bounding hypercube. In fact, even if each parameter κ_i can be bounded to the interval $[\kappa_i^{\min}, \kappa_i^{\max}]$, there are a number of relations among κ_is that come from basic circui t operating conditions. The exploitation of these constraints is very important to properly bias sampling so that approximations of $\mathcal{P}$ be obtained more efficiently. Of course, in non-degenerate cases the $n + m$ constraints underdetermine the value of κ, but determine a space $\mathcal{I}_{eff}$ whose size is much smaller than the hypercube $\prod[\kappa_i^{\min}, \kappa_i^{\max}]$ (Cartesian product).

3. EXAMPLE: WCDMA AMPLIFIER

In this section we show a simple example of analog platform driven exploration on a low noise amplifier for an ultra-wideband CDMA amplifier. The amplifier is based on a cascade of simple gain stages. The basic schematic is reported in Fig. 1. The technology used is a $0.13\mu m$ CMOS. Since the overall amplifier is going to operate in an open-loop configuration, a g_m-g_m topology is selected for each stage so that gain does not depend much on process corners. The circuit biasing conditions are (assuming perfect matching on the differential paths):

$$\begin{cases} I_B = I_{D_1} = 2I_{D_2} = 2(I_{D_4} + I_{D_6}) & \textit{current sharing} \\ \sum (V_{GS_i} - V_T) < V_{DD} & \textit{saturation} \\ I_D = k\frac{W}{L}\frac{(V_{GS}-V_T)^2}{1+\frac{V_{GS}}{\xi_c L}} & \textit{short channel} \end{cases} \quad (1)$$

The small signal gain is $G = \frac{g_{m_2}}{g_{m_4} - g_{m_6}}$ with the condition $g_{m_6} < g_{m_4}$. Using again the long channel approximation, the ratio g_{m_6}/g_{m_4} is equal to $\frac{W_6 L_4}{L_6 W_4}$ which is controlled by the ancillary variable χ in the ACG in Fig. 1.

A platform encapsulation has been derived for the single amplifying stage. The loading effect of the next stage has been implicitly included in the model parameters considering C_L. The considered performance figures $\zeta \in \mathcal{O}$ include $\{C_{in}$, *gain, bandwidth, noise (RMS), power,* $C_L\}$. The configuration parameters $\kappa \in \mathcal{I}$ include $\{ I_{bias}, W_1, L_1, W_2, L_2, W_3, L_3, W_5, L_5\}$. The evaluation function $\phi(\cdot)$ is a Spectre simulation. An ACG has been set up to generate an approximation for $\mathcal{P}_{g_m}$. A set of relations on configuration parameters is derived to specify necessary conditions for correct biasing. Conditions on gain and bandwidth are included as well to further refine the sampling space $\mathcal{I}$.

Stage	*Power*	*noise*	*BW*	*gain*
3	$158\mu W$	$2.9mV$	$2.8GHz$	28
4	$210\mu W$	$3.3mV$	$2.4GHz$	26
5	$312\mu W$	$6.5mV$	$2.5GHz$	33

Table 2: Optimization results as a function of the number of stages. The minimum power design consists of 3 stages. The 4 stage design exhibits lower bandwidth and gain performances to minimize noise, while 5 stages have definitely larger noise and power consumption.

The exploration objective is to find over the feasible performances of each stage, the best combination of number of stages and stage specifications so as to minimize power and noise subject to gain and bandwidth constraints. The optimization has been carried out with simulated annealing with the results shown in table 2. Optimization took 20 minutes on a 700 MHz Pentium III. In order to provide initial designs for an eventual circuit level optimization, the designs with closest performances to the requested κ have been selected in the approximation database. As reported in table 1, the estimated performances are within 2 (average) to 5% (maximum) of the range of variability of single performance figures.

4. CONCLUSIONS

In this paper a new approach to analog system level design has been proposed. The extension of the platform concept to the analog world is very smooth and provides a formal framework to quantitatively address complex issues at the system level. By decoupling circuit design from system assembly, analog designers are not limited to a particular set of topologies or architectures, so that the approach can be easily adopted in different design flows/habits.

5. REFERENCES

[1] A. Sangiovanni-Vincentelli, "Defining platform-based design," *EE-Design*, March 2002.

[2] L. Carloni, F. De Bernardinis, A. Sangiovanni Vincentelli, and M. Sgroi, "The art and science of integrated systems design," in *Proceedings of ESSCIRC'02*, pp. 25–36, September 2002.

[3] H. Liu, A. Singhee, R. Rutenbar, and L. R. Carley, "Remembrance of circuits past: Macromodeling by data mining in large analog design spaces," in *Proceedings of DAC*, 2002.

[4] F. D. Bernardinis, M. Jordan, and A. S. Vincentelli, "Support vector machines for analog circuit performance representation," in *Proc. of DAC*, June 2003.