Diagnosis of Scan-Chains by Use of a Configurable Signature Register and Error-Correcting Codes

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Abstract

In this paper a new diagnosis method for scan designs with many scan-paths based on error correcting linear block codes with N information bits and K control bits is proposed, where N is the number of scan-paths. The new approach can be implemented on a modified STUMPS-architecture. In diagnosis mode the test has K times to be repeated. In the K repetitions of the test the outputs of the scan-paths are connected to a configurable signature register (with disconnected feedback logic) according to the coefficients of the K syndrome equations of the code. By monitoring the one-dimensional output sequence of the configurable signature register the failing scan-cells in the different scan-paths can be identified with the resolution of the selected error correcting code. Since for the relevant codes, e.g.(shortened) Hamming codes, T-error correcting BCH-code, the ratio $\frac{K}{N}$ decreases very fast with an increasing number N the method is useful for a large number of scan-paths.

1. Introduction

Scan design is accepted as an industrial standard for test. The number of scan-cells in a chip are tremendously increasing every year and hundreds of scan-paths with hundreds of scan-cells in industrial designs are reality.

In this paper we describe the basic principles of a new diagnosis method for large scan designs. After giving an introduction into the test architecture and an overview of prior work in chapter 2, in chapter 3 some basic notions of linear systematic error correcting codes are recapitulated and illustrated for a error correcting code with 4 information bits and 3 control bits.

In Chapter 4 the proposed diagnosis method is explained on the example of a Hamming-code. In chapter 5 the advantages of the proposed diagnosis method in an industrial environment are discussed. In chapter 6 conclusions are drawn.

2. Introduction into test architecture and reference to prior work

The well-known STUMPS-architecture [1],[2] which is widely used as a test architecture for scan designs is slightly modified as shown in Fig.1 .

The outputs of N scan-paths with L scan-cells are connected to the N inputs of a $MISR$ via N controlled AND-gates. For the control signals $d_1 = 1$ (0) and $d_2 = 1$ the feedback logic of the MISR is active (not active). The Test Input Generator TIG generates pseudorandom test inputs, pseudorandom test inputs with embedded deterministic test vectors or deterministic test vectors [2],[5],[3],[4]. In test mode the test input generator fills the N scan-paths. The contents of the scan-paths are applied to the combinational part of the circuit under test (not shown in Fig. 1) and the test results are captured in the scan-paths and shifted out. The outputs of the scan-paths are compacted by the MISR with an active feedback logic and the control signals $c_0, \cdots, c_{N-1}$ set to 1.

For the simplicity of presentation it is assumed that the N scan-paths in Fig. 1 consist of L scan-cells each. Different lengths of the scan paths can also easily be handled [2]. When the entire circuit test as a sequence of multiple scan test cycles is completed the signature of the MISR will be evaluated. An erroneous signature indicates a faulty circuit under test and as first step the erroneous scan-cells have to be diagnosed. If the circuit under test is identified as faulty the scan-paths $S_0, \cdots, S_{N-1}$ in the STUMPS-architecture can be serially connected into a single scan-path [2] or into several scan-paths [9] to shift out the test results and to identify the erroneous scan-cells. For a large number of flip-flops this approach is very time-consuming and a large

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memory to store all these test results is needed.

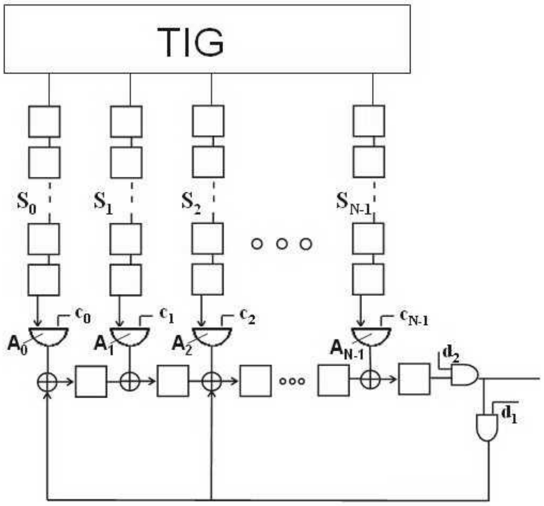

Figure 1. : Modified STUMPS-architecture

To reduce time and memory requirements for diagnosis there are many proposals to conclude from the erroneous signature(s) of the MISR to the failing scan-cells [10], [11], [12]. Usually one scan-path is considered in these solutions. In [7], [8] the scan-cells are partitioned to remove as fault-free identified scan-cells from the potential fault list. A solution for a relatively small number of scan-paths is described in [13]. Here frames of scan-cells can be identified. In order to identify up to t erroneous frames the test has $2t$ times to be repeated using $2t$ different primitive feedback polynomials which are to be realized in hardware. To localize instead of frames failing scan-cells every scan-path has to be considered separately. For a large numbers of scan-paths this will be expensive.

This work focuses on a new solution which is suited for diagnosing large designs consisting of many hundred scan paths during production test. Such new solution has to provide an exact identification of the failing scan-cells with only small overhead in test time and data. It is shown how to identify the erroneous scan cells of the different scan-paths by use of an arbitrary linear systematic error correcting code with N information bits and K control bits. The desired diagnostic resolution which is to a large extend determined by the number K of control bits and the apropriate code can be specified at diagnosis runtime. As already pointed out, the well-known STUMPS-architecture can be used.

In diagnosis mode the feedback of the MISR is disconnected and the MISR is transformed into a shift-register with N parallel inputs without feedback. The 1-dimensional output of this shift register is monitored. The number of symptom equations of the considered error-correcting code, which is equal to the number K of control bits, determines how often the same test has to be repeated for diagnosis. The outputs of the scan-paths are connected to or disconnected from the MISR in the successive repetitions of the test in accordance to the linear symptom equations of the code. By selecting an appropriate code the method can be easily adapted to different diagnostic resolutions.

To do so only the number of repetitions of the test and the values of the control signals of the masking AND-gates, but not the test architecture itself has to be adapted to the desired resolution.

3. Linear Error Correcting Codes

In this chapter we recapitulate some of the basic notations of systematic error correcting linear block-codes which are needed for the description of the proposed diagnosis method. Linear error detecting and correcting block-codes are for instance described in [14], [15].

In a linear block code N information bits $y_0, \cdots, y_{N-1}$ and K control bits $z_0. \cdots, z_{K-1}$ are forming the code-word blocks $v_0, v_1, \cdots, v_{N+K-1} = z_0, \cdots, z_{K-1}, y_0, \cdots, y_{N-1}$ of $N + K$ bits.

For $i = 0, \cdots, K-1$ the control bit z_i is determined by the linear equation

$$z_i = p_{i,0}y_0 \oplus p_{i,1}y_1 \oplus \cdots \oplus p_{i,N-1}y_{N-1} \qquad (1)$$

where the coefficients $p_{i,j} \in \{0, 1\}$ for $0 \leq i \leq K-1$ and $0 \leq j \leq N-1$ are the elements of the (N, K) parity matrix $\mathbf{P}_{K,N}$ of the code. For the proposed application only a subset of the information bits $y_0, \cdots, y_{N-1}$ of a code word, but not the control bits, can be erroneously changed into $\tilde{y}_0 = y_0 \oplus e_0, \cdots, \tilde{y}_{N-1} = y_{N-1} \oplus e_{N-1}$, where $e = e_0, \cdots, e_{N-1}$ is the binary error vector of the information bits. For erroneous information bits we obtain by substituting y_i by $\tilde{y}_i$ in (1)

$\tilde{z}_i = p_{i,0}\tilde{y}_0 \oplus p_{i,1}\tilde{y}_1 \oplus \cdots \oplus p_{i,N-1}\tilde{y}_{N-1}$
$= p_{i,0}(y_0 \oplus e_0) \oplus p_{i,1}(y_1 \oplus e_1) \oplus \cdots \oplus p_{i,N-1}(y_{N-1} \oplus e_{N-1})$
$= z_i \oplus p_{i,0}e_0 \oplus p_{i,1}e_1 \oplus \cdots \oplus p_{i,N-1}e_{N-1}$
or

$$s_i = \tilde{z}_i \oplus z_i = p_{i,0}e_0 \oplus p_1e_1 \oplus \cdots \oplus p_{i,N-1}e_{N-1}, \quad (2)$$

where s_i is called the ith component of the syndrome $s = s_0, \cdots, s_{N-1}$ of the error $e = (e_0, \cdots, e_{N-1})$. For $i = 0, \cdots, N-1$ the components s_i of the syndrome of an arbitrary error $e = (e_0, \cdots, e_{N-1})$ in the information bits are equal to the XOR-sum of the corresponding control bits $\tilde{z}_i$ and z_i, where $\tilde{z}_i$ is determined from the erroneous and z_i

from the error free information bits of the code words. Obviously the syndrome is $(0, \cdots, 0)$ if no error occurs.

Let us assume that only a specific subset of M errors $\{e^1, e^2, \cdots, e^M\}$ of all possible 2^N errors occurs. This is e.g. the case if only a limited number of the N information bits will be erroneous. For single bit errors we have $M = N$ and the corresponding subset of error vectors is $\{e^1 = (1, 0, \cdots, 0), e^2 = (0, 1, \cdots, 0), \cdots, e^N = (0, \cdots, 0, 1)\}$.

According to equation (2) for every error vector $e^j, j = 1, \cdots, M$ of the considered subset of errors a syndrome $s^j = (s^j_0, \cdots, s^j_{N-1})$ is determined. If for all different error vectors all corresponding syndromes are mutually different then the error vector is uniquely determined by the syndrome. Hence the error vector determines which bit positions of the information bits are erroneous. Such a code is called error correcting.

We illustrate now the described equations for a Hamming-code with 4 information bits r, s, t, u and 3 control bits z_1, z_2, z_3 :

$$z_0 = r \oplus s \oplus t,\ z_1 = r \oplus s \oplus u,\ z_2 = r \oplus t \oplus u. \tag{3}$$

If the information bits r, s, t, u are changed into $(\tilde{r}, \tilde{s}, \tilde{t}, \tilde{u}) = (r \oplus e_0, s \oplus e_1, t \oplus e_2, u \oplus e_3)$ we have

$$\tilde{z}_0 = \tilde{r} \oplus \tilde{s} \oplus \tilde{t} = r \oplus e_0 \oplus s \oplus e_1 \oplus t \oplus e_3 = z_0 \oplus e_0 \oplus e_1 \oplus e_2$$
$$\tilde{z}_1 = \tilde{r} \oplus \tilde{t} \oplus \tilde{u} = z_1 \oplus e_0 \oplus e_1 \oplus e_3$$
$$\tilde{z}_2 = \tilde{r} \oplus \tilde{t} \oplus u = z_2 \oplus e_0 \oplus e_2 \oplus e_3$$

or

$$s_0 = z_0 \oplus \tilde{z}_0 = e_0 \oplus e_1 \oplus e_2$$
$$s_1 = z_1 \oplus \tilde{z}_1 = e_0 \oplus e_1 \oplus e_3$$
$$s_2 = z_2 \oplus \tilde{z}_2 = e_0 \oplus e_2 \oplus e_3.$$

All the possible 1-bit errors in the information bits can be described by the four error vectors $(1, 0, 0, 0)$, $(0, 1, 0, 0)$, $(0, 0, 1, 0)$,$(0, 0, 0, 1)$. These error vectors are mapped to the syndroms $(1, 1, 1)$, $(1, 1, 0)$, $(1, 0, 1)$ and $(0, 1, 1)$ which are all different.

Thus, if we know the differences $z_i \oplus \tilde{z}_i, i = 1, 2, 3$ of the control bits computed from the correct and from the erroneous information bits then the corresponding error vector is uniquely determined and the erroneous bit positions in the information bits are identified. A Hamming code with $N = 4$ information bits and $K = 3$ control bits is of course not relevant for the proposed diagnosis method. In general, the number of information bits which can be checked by K control bits of an error correcting Hamming code is determined by $N = 2^K - k - 1$. Hence, for example up to 502 information bits can be checked by $K = 9$ control bits. If not all the information bits are used the code is called a shortened code [14], [15].

4. Description of the Proposed Diagnosis Method

In this section we exemplify how the erroneous scan-cells in the different scan-paths can be diagnosed by use of a linear error-correcting code.

In Fig. 2 $N = 4$ scan-paths of 5 scan-cells are connected to a MISR of $N = 4$ flip-flops D_0, D_1, D_2 and D_3. After the application of the ith test vector the corresponding test responses $u^i_1, u^i_2, \cdots, u^i_5$; $v^i_1, v^i_2, \cdots, v^i_5$; $t^i_1, t^i_2, \cdots, t^i_5$; $s^i_1, s^i_2, \cdots, s^i_5$; $r^i_1, r^i_2, \cdots, r^i_5$ of the circuit under test are captured in the scan-paths $S_0, \cdots, S_3$.

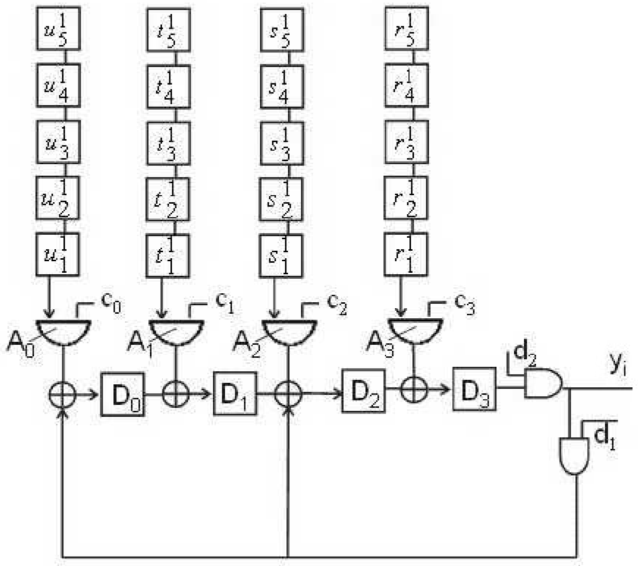

Figure 2. : Example circuit

In Fig. 2 the corresponding values for the first test vector are shown. During test we have for the control signals $d_1 = d_2 = 1, c_0 = c_1 = c_2 = c_3 = 1$ and a signature is accumulated in the memory elements D_0, D_1, D_2 and D_3. In diagnosis mode the feedback logic is disconnected by setting $d_1 = 0$. The control signals c_0, c_1, c_2, c_3 of the masking AND-gates A_0, A_1, A_2, A_3 are selected according to the proposed diagnosis algorithm. With $d_2 = 1$ the output of D_3 can be observed as the output y_i. We assume that the initial state of all the memory elements of the MISR is 0.

For fixed values of $c = (c_0, c_1, c_2, c_3)$ we result for the first outputs

$(y_0 = 0)$
$y_1(c) = c_3 r_1^1$
$y_2(c) = c_3 r_2^1 \oplus c_2 s_1^1$
$y_3(c) = c_3 r_3^1 \oplus c_2 s_2^1 \oplus c_1 t_1^1$
$y_4(c) = c_3 r_4^1 \oplus c_2 s_3^1 \oplus c_1 t_2^1 \oplus c_0 u_1^1$
$y_5(c) = c_3 r_5^1 \oplus c_2 s_4^1 \oplus c_1 t_3^1 \oplus c_0 u_2^1$
$y_6(c) = c_3 r_1^2 \oplus c_2 s_5^1 \oplus c_1 t_4^1 \oplus c_0 u_3^1$
$y_7(c) = c_3 r_2^2 \oplus c_2 s_1^2 \oplus c_1 t_5^1 \oplus c_0 u_4^1$
$\vdots$

In compact form this can be written as

$$y(c_0, c_1, c_2, c_3) = c_3 r \oplus c_2 s \oplus c_1 t \oplus c_0 u \tag{4}$$

where r, s, t, u and y denote the column vectors
$r = [r_1^1,\ r_2^1,\ r_3^1,\ r_4^1,\ r_5^1,\ r_1^2,\ r_2^2,\ r_3^2,\ \cdots]^T$,
$s = [0\ \ , s_1^1,\ s_2^1,\ s_3^1,\ s_4^1,\ s_5^1,\ s_1^2,\ s_2^2,\ \cdots\ ]^T$,
$t = [0,\ \ 0,\ \ t_1^1,\ t_2^1,\ t_3^1,\ t_4^1,\ t_5^1,\ t_1^2,\ \cdots\ ]^T$,
$u = [0,\ \ 0,\ \ 0,\ \ u_1^1,\ u_2^1,\ u_3^1,\ u_4^1,\ u_5^1,\ \cdots\ ]^T$
$y(c) = [y_1(c),\ y_2(c),\ y_3(c),\ \cdots\ ]^T$.

Now consider the four bit words $[r_1^1, 0,\ 0.\ 0,\ ]$, $[r_2^1, s_1^1, 0,\ 0,\ ]$, $[r_3^1, s_2^1, t_1^1, 0\ ]$, $[r_4^1, s_3^1, t_2^1, u_1^1]$, $[r_5^1, s_4^1, t_3^1, u_2^1]$, $[r_1^2, s_5^1, t_4^1, u_3^1]$, $[r_2^2, s_1^2, t_5^1, u_4^1] \cdots$ as the information bits (compare to equations for $y_0, y_1, y_2, ...$) of an error correcting Hamming code with four information bits and three control bits.

Since the number of control bits is $K = 3$ the test has three times to be repeated. For the repeated applications of the test we select the control signals c_0, c_1, c_2, c_3 in accordance with the coefficients of the three equations of the control bits.

In equation (3) the first control bit z_0 is determined as $z_0 = s \oplus t \oplus u$. Thus the control signals for the first test are $c_0 = 1,\ c_1 = 1,\ c_2 = 1,\ c_3 = 0$. Since the second control bit z_1 is determined as $z_1 = r \oplus t \oplus u$, for the second application of the test the control signals are to be set to $c_0 = 1,\ c_1 = 1,\ c_2 = 0,\ c_3 = 1$. For the third control bit z_2 we have $z_2 = r \oplus s \oplus u$ and the control signals $c_0 = 1, c_1 = 0, c_2 = 1, c_3 = 1$. In the three diagnosis runs $y_1(c),\ y_2(c),\ y_3(c),\ y_4(c),\ y_5(c),\ y_6(c),\ y_7(c),\ \cdots$ will be the control bits of the corresponding information bits.

As we have explained in section 3 the syndromes $s_i = (s_i^1, s_i^2, s_i^3)$ are the XOR-sums of the control bits of the correct circuit under test and the faulty circuit under test. In this example we have

$s_i^1 = y_i(1,\ 1,\ 1,\ 0) \oplus \tilde{y}_i(1,\ 1,\ 1,\ 0)$
$s_i^2 = y_i(1,\ 1,\ 0,\ 1) \oplus \tilde{y}_i(1,\ 1,\ 0,\ 1)$
$s_i^3 = y_i(1,\ 0,\ 1,\ 1) \oplus \tilde{y}_i(1,\ 1,\ 0,\ 1)$

where the one-dimensional outputs of the MISR without feedback for the correct and erroneous circuit under test are denoted by $y_i(c)$ and $\tilde{y}_i(c)$ with $c = (c_0, c_1, c_2, c_3)$. If e.g. now we have $s_1 = s_2 = s_3 = (0,0,0)$, $s_4 = (1,1,0)$, $s_5 = (0,0,0)$, $s_6 = (1,1,1)$ and $s_7 = (1,1,1)$.Then the corresponding error vectors of these syndromes, as described in chapter 2, are $e_1 = e_2 = e_3 = e_5 = (0,\ 0,\ 0,\ 0\ )$, $e_4 = (\ 0,\ 1,\ 0,\ 0\ )$, $e_6 = (\ 1,\ 0,\ 0,\ 0\ )$ and $e_7 = (\ 1,\ 0,\ 0,\ 0\ )$. The data words $[r_4^1, s_3^1, t_2^1, u_1^1]$, $[r_1^2, s_5^1, t_4^1, u_3^1]$ and $[r_2^2, s_1^2, t_5^1, u_4^1]$ are erroneously changed into $[r_4^1, \overline{s}_3^1, t_2^1, u_1^1]$, $[\overline{r}_1^2, s_5^1, t_4^1, u_3^1]$ and $[\overline{r}_2^2, s_1^2, t_5^1, u_4^1]$. In the scan path S_3 two failing scan-cells, r_1^2 and r_2^2, are correctly identified as erroneous. In this example and also in the general case, a large number of failing scan-cells can be identified. If a Hamming code is applied, the only restriction is that ther must not be two failing scan cells in the same N-bit data word which is located in a " diagonal" orientation in the scan-paths. If this condition is not acceptable a t-error correcting linear block code, for instance a BCH-code [14] has to be used. Then also up to t failing scan-cells in one "diagonals" can be identified. Undefined values in the scan-cells can also be tolerated by this method. If an undefined value (X-value) is shifted out at the scan-path S_i at time t either the control signal c_i of the AND-gate A_i at time t or the control signal d_2 at time $t + N - i$ has to be zero.

5. Application of the diagnosis method in an industrial environment

For diagnosis during production test the diagnosis test time, the data to be stored and the requirements on the test system are to be minimized.

A favorable implementation of the proposed method in an industrial environment is to use the signature register without feedback already in the first test run and a Hamming-Code for calculating the erroneous scan-cells. During the first run the MSBs coming out of the shift register are to be compared to the expected test values. In case of a mismatch of the MSB the corresponding cycle number is to be stored. At the failing cycle numbers the control bits of the Hamming code for the corresponding failure will be shifted out in the subsequent test runs. Only the bits on these positions need to be stored in the tester and the data volume for diagnosing the erroneous scan cells is significantly reduced to $F * log(N)$ where N is the number of scan-chains and F the number of failing scan-cells to be diagnosed. F depends on the algorithm which is applied to calculate the failing node in a later step.

To demonstrate the advantages of the proposed method this method is compared to a diagnosis method for a large industrial chip which we call standard method. This is because alternative solutions are rather targeted to labaratory diagnosis than to production test. In this method the MSB of a MISR without feedback is observed also during test. If a mismatch at time t occurs the erroneous MSB was potentially caused by the erroneous output of the kth scan-path, $k = 0, \cdots, N-1$ at time $t - (N - k)$. This is true if an odd number of the scan-cells forming such a "diagonal" in the scan-paths $S_0, \cdots, S_{N-1}$ is erroneous. To guarantee a "tough" comparison of the standard method with the proposed method we assume that in the standard method it is possible to scan out only the captured test responses of the scan-cells which are located in the "faulty diagonal". The scan-out of the potentially faulty bits is done in subsequent scan-pattern runs with individual initialization of the tester for each of the F failures.(This can for instance be done by an appropriate masking of the outputs of the scan-paths and reducing the clock frequency for scan-shift to $\frac{1}{2}$ of the clock frequency of the MISR or by an appropriate masking of the outputs of the scan-paths and by use of a bidirectional MISR without reducing the clock rate for scan-shift.)

The chip which is to be diagnosed consists of 500000 flip-flops, which are partitioned into $N = 2000$ scan-chains of 250 Scan FF. As it can be expected that the diagnosis algorithm used in an industrial environment won't need the complete fail information of the chip, maybe to the cost of a reduced resolution [18], the first 100 test vectors are used for diagnosing the chip. For this first 100 scan loads the erroneous scan cells have to be determined. If the diagnostic resolution using the fail information of these 100 test inputs is not good enough, the remaining erroneous scan cells can be diagnosed using a specialized method for few fails like e.g. proposed in [19].

Let us assume that the testing of two chips is always dependent because of limited resources on the ATE equipment. This could be e.g. because the number of test pattern generators is smaller than the number of chips tested in parallel. The two chips then will always be stimulated with the same input sequence, which is no limitation during normal test. Having a shift frequency of 50 MHz the time to run 100 Scan loads is 0.5 ms. For a pattern start on the ATE an ATE dependent overhead of 1 ms (0 ms) is assumed. If e.g. 20 fails are to be detected in the 100 scan loads, the standard method will need 20 pattern restarts per device. Because of individual initialization per failure the two dependent chips diagnosis can only be done serially, thus 40 pattern restarts are necessary. It is approximated that in average the failing bits will be read out in the middle of the 100 Scan loads. The pattern can be aborted after an erroneous readout. Hence for diagnosing using the standard method 40*1.25 ms=50 ms (40*0.25ms= 10 ms) are needed, additionally per device 20*2000=40000 bits are to be read out of the tester memory. Some testers will need a special device to store this amount of data.

The proposed method using a (shortened) Hamming-Code with N=2000 information bits needs K= 11 control bits for calculating the errors, K=11 subsequent test runs respectively. Thus the data volume to be stored by the production tester is reduced significantly to F*log(N)=20*11=220 bits. The 11 pattern restarts need 11*1.5 ms = 16.5 ms (11*0.5 ms = 5.5 ms).

The depending chips can be diagnosed in parallel as the proposed method is not failure dependent. It can be seen that the proposed diagnosis method is very well suited for data acquisition during high volume production testing, as requirements on test instrumentation and test time are very low.

Further improvements of the proposed approach could be e.g. to choose depending on the number of mismatches in the first run an appropriate error correction code to reduce the probability of aliasing. Alternatively an algorithm respecting potential aliasing effects of the error-correction code in the ATPG diagnosis software will turn the application of a more complex error correction code unnecessary.

6. Conclusions

In this paper the basic principle of a new diagnosis method for full-scan designs with many scan-paths was proposed. The method is based on the application of arbitrary error correcting linear block codes with N information bits and K control bits. N is equal to the number of scan-paths. In test- and diagnosis modes the (slightly modified) STUMPS-architecture can be used. If in test mode the circuit under test was identified as erroneous in the following diagnosis mode the test has K times to be repeated. In these K repetitions of the test the outputs of the scan-paths are connected to the MISR-compactor (with disconnected feedback logic) according to the coefficients of the K different syndrome equations of the code. By monitoring the one-dimensional output sequence of the MISR the failing scan-cells in the different scan-paths can be identified with the resolution of the selected error correcting code which is basically determined by the number K of control bits. Since for the appropriate codes [(shortened) Hamming codes, t-error correcting BCH-codes]the ratio $\frac{K}{N}$ decreases very fast with an increasing number N of information bits the method is useful for a large number of scan-paths.

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References

[1] Bardell,P., and McAnney, W.:Self-Testing of Multichip Logic Modules, ITC 1982, pp. 200-204.

[2] Bardell,P., McAnney,W., Savir,J.,: Built-In Test for VLSI: Pseudorandom techniques,Wiley, NY, 1987.

[3] Wunderlich, H., J. and Kiefer, G.: Bit-Flipping BIST, Proc. ICCAD, San Jose, 1996, pp. 337-343

[4] Kiefer,G. and Wunderlich, H.,J.: Deterministic BIST with Multiple Scan-Chains, Proc. ITC,Wahington, 1998, pp. 1057-1064.

[5] Rajski,J.,Tamarapilli,N., and Tyszer,J.:Automated synthesis of phase shifters for built-in self-test applications. IEEEtrans. CAD, 19, pp.1175-1188, 2000.

[6] Savir,J., and McAnney,W.,: Identification of Failing Tests with Cyclic Registers, ITC pp. 322-328.

[7] Bayraktaroglu, I. and Orialoglu, A. : Improved Fault Diagnosis in Scan-Based BIST via Superposition, Proc. DAC, Los Angeles, 2000, pp.

[8] Rajski, J. and Tyscer,J.: Diagnosis of scan-cells in BIST environment. IEEE Trans. Comp. vol 48, pp. 724-731, 1999

[9] Hsu,F.,Nutler,K and Patel,J. : A case study on the implementation of the Illinois Scan Architecture, ITC 2001, pp. 538-547

[10] Savir, J., and McAnney, W.: Identification of Failing Tests with Cyclic Registers, ITC, pp 322-328, 1988.

[11] Karpovsky, M., and Chaudry, S.,: Design of Self-Diagnosing Boards by Multiple Signature Analysis. IEEE trans. Comp. 42, pp. 1035-1044, 1993.

[12] Damarla, T., Stroud, C., and Sathaye, A.: Multiple Error Detection and Identification via Signature Analysis, JETTA, 7, pp 193-207, 1995.

[13] Wu, Y., and Adham,S.,: Scan-based BIST Fault Diagnosis, IEEE trans. CAD, 18, pp 203-211, 1999.

[14] Lin,S., and Costello,J.: Error Control Coding,Prentice-Hall, 1983.

[15] Rao,T., and Fujiwara,E.: Error Control Coding for Computer Systems, Prentice Hall, N.Y., 1989.

[16] Rajski,J. at all,: Embedded Deterministic Test for Low Cost Manufacturing Test. ITC, pp. 301-310, 2002.

[17] Rajski,J., Tyszer,J., Fault Diagnosis in Scan-Based BIST, ITC pp. 894-902, 1997.

[18] C.Hora, R.Segers, S.Eichenberger, M.Lousberg : On a statistical fault diagnosis approach enabling fast yield ram-up, ETW, pp.193-198, 2002

[19] M. Goessel, K. Chakrabarty, V. Otscheretnij, A. Leininger: Identification of Failing Vectors using Signature Analysis with Application to Scan-BIST, DDECS Workshop Poznan, IEEE Pres. pp. 81-86 2003.

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