Hybrid Delay Scan: A Low Hardware Overhead Scan-based Delay Test Technique for High Fault Coverage and Compact Test Sets

Seongmoon Wang
NEC Labs., America, Princeton, NJ
swang@nec-labs.com

Xiao Liu
Virginia Tech.
liux@visc.vt.edu

Srimat T. Chakradhar
NEC Labs., America, Princeton, NJ
chak@nec-labs.com

Abstract

A novel scan-based delay test approach, referred as the hybrid delay scan, is proposed in this paper. The proposed scan-based delay testing method combines advantages of the skewed-load and broad-side approaches. Unlike the skewed-load approach whose design requirement is often too costly to meet due to the fast switching scan enable signal, the hybrid delay scan does not require a strong buffer or buffer tree to drive the fast switching scan enable signal. Hardware overhead added to standard scan designs to implement the hybrid approach is negligible. Since the fast scan enable signal is internally generated, no external pin is required. Transition delay fault coverage achieved by the hybrid approach is equal to or higher than that achieved by the broad-side load for all ISCAS 89 benchmark circuits. On an average, about 4.5% improvement in fault coverage is obtained by the hybrid approach over the broad-side approach.

1. Introduction

With ever decreasing geometry sizes and increasing clock speeds, ascertaining correct operation of digital circuits at desired speed is becoming a necessity rather than an option to maintain high product quality level. However, developing functional test patterns that attain satisfactory fault coverage is unacceptable for large scale designs due to the prohibitive development cost. Even if functional test patterns that can achieve high fault coverage are available, applying these test patterns at-speed for high speed chips requires very stringent timing accuracy, which can be provided by very expensive automatic test equipments (ATEs). The scan-based delay testing where test patterns are generated by an automatic test pattern generator (ATPG) on designs that involve scan chains is increasingly used as a cost efficient alternative to the at-speed functional pattern approach to test large scale chips for performance-related failures [1, 12]. Design-for-testability (DFT)-focused ATEs [3, 8], which are designed to lower ATE cost by considering widely used DFT features of circuits under test (CUTs) such as full and partial scan, are emerging as a strong trend in test industry.

Detecting a delay fault normally requires the application of a pair of test patterns: the first pattern, called *initialization pattern*, initializes the targeted faulty circuit line to a desired value and the second pattern, called *launch pattern*, launches a transition at the circuit line and propagates the fault effect to primary output(s) and/or scan flip-flop(s). Traditionally, two different approaches, the *skewed-load approach* and the *broad-side approach*, have been used to apply two-pattern tests to standard scan designs. They differ in the way of applying the second pattern of each pattern pair (see Section 2).

In this paper, we present a novel scan-based delay test approach that combines advantages of the skewed-load and broad-side approaches. In the proposed approach, only a small set of selected scan flip-flops are controlled by the skewed-load approach and the rest of scan flip-flops are controlled by the broad-side approach. Hardware overhead to implement the proposed technique is comparable to that for the traditional broad-side approach. The proposed approach can achieve higher fault coverage than the traditional broad-side approach with smaller test set sizes. Although the proposed technique is applicable to other delay fault models, in this paper we focus only on transition delay fault model [13].

The rest of this paper is organized as follows. General scan-based delay testing methods are explained in Section 2. The motivation and key idea of the proposed hybrid approach are described in Section 3. The selection criterion used to select the flip-flops to be controlled by the skewed-load approach is described in Section 4. A circuit to generate the fast scan enable signal that drives flip-flops controlled by the skewed-load approach is presented in Section 5. Section 6 reports experimental results. Finally, Section 7 gives the conclusions.

2. Scan-Based Delay Testing

When a sequential circuit employs full scan, test pattern pairs for transition delay faults can be generated by run-

1530-1591/04 $20.00 (c) 2004 IEEE

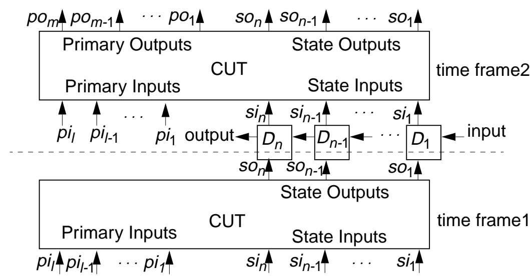

Figure 1. Two Frame Version Full-Scan Circuit

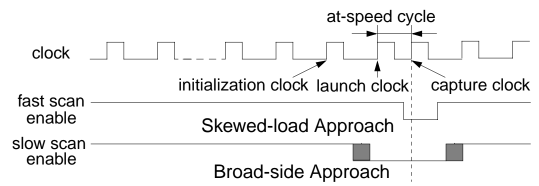

Figure 2. Scan-based Test Timing Diagram

ning a combinational ATPG on a two time frame version of the circuit. A two time frame version of a sequential circuit that employs full scan is shown in Figure 1. The circuit has l primary inputs, $pi_1, pi_2, \ldots, pi_l$, m primary outputs, $po_1, po_2, \ldots, po_m$, n state inputs, $si_1, si_2, \ldots, si_n$, and also n state outputs, $so_1, so_2, \ldots, so_n$. State outputs so_i, where $i = 1, 2, \ldots, n$, of the first time frame copy are connected to state inputs si_i of the second time frame copy. In the original circuit, the pair of state output so_i and state input si_i are connected through a scan flip-flop D_i to constitute a feedback loop. All scan flip-flops are controlled by scan enable signal(s) to configure them into either their shift mode or normal mode. We assume that the scan chain is constructed with muxed scan type flip-flops (see Figure 4).

Test procedures of the two traditional approaches to apply test pattern pairs to standard scan designs are illustrated in the timing diagrams shown in Figure 2. In both skewed-load and broad-side approaches, the initialization pattern of a test pattern pair is first loaded into the scan chain by n consecutive *scan shift operations*, where n is the number of scan flip-flops in the scan chain. The clock speed during scan shift operations is typically lower than the full system clock speed. The launch pattern is applied after the CUT is stabilized from switching caused by applying the initialization pattern. The response to the launch pattern is captured into scan flip-flops at the next clock cycle.

In the skewed-load approach [10], the second pattern of each pattern pair is obtained by shifting in the first pattern (initialization pattern) by one more scan flip-flop and scanning in a new value into the scan chain input. The scan enable signal, which is at logic high during the launch cycle, then switches to logic low to configure scan flip-flops into their normal mode at the next clock cycle (capture cycle). Since the capture clock is applied at the full system clock speed after the launch clock, the scan enable signal, which typically drives all scan flip-flops in the CUT, should also switch in the full system clock cycle. This requires the scan enable signal to be driven by a sophisticated buffer tree or strong clock buffer. Such a design requirement is often too costly to meet. Furthermore, meeting such a strict timing requirement for the scan enable signal may result in longer design time.

Since the second pattern of each pattern pair is obtained by shifting in the first pattern by one more scan flip-flop, given a first pattern, there are only two possible patterns for the second pattern that differ only at the value for the first scan flip-flop whose scan input is connected to the scan chain input. Due to this *shift dependency*, if there is a transition delay fault that requires a 1 at state input si_{i-1} in an initialization pattern and requires a 0 at state input si_i in the corresponding launch pattern to be detected, then that fault is *shift dependency untestable* (assume that the scan chain is constructed by using only non-inverting outputs of scan flip-flops).

In the broad-side approach, the second pattern is obtained from the circuit response to the first pattern. Hence, the scan flip-flops are configured into their normal mode by lowering the scan enable signal before every launch cycle (see Figure 2). Since the launch clock following the initialization clock need not be an at-speed clock, the scan enable signal does not have to switch to logic low at the full system clock speed between the initialization clock and the launch clock. Note that the scan enable signal does not switch during the at-speed cycle, i.e., between the launch and capture clocks. Therefore, the broad-side approach does not require at-speed switching capability for the scan enable signal.

Since in the broad-side approach, the second pattern is given by the circuit response to the first pattern, unless the circuit can switch to all 2^n states, where n is the number of scan flip-flops, the number of possible patterns that can be applied as second patterns of test pattern pairs is limited. Hence, if a state required to activate and propagate a transition delay fault is an invalid state, then the fault is *function dependency untestable*.

Even though the broad-side approach is cheaper to implement than the skewed-load approach, fault coverage achieved by the broad-side approach is typically lower than that achieved by the skewed-load approach [11]. Test pattern sets generated by the broad-side approach are also typically larger than those generated by the skewed-load approach [12]. In order to generate two pattern tests by the broad-side approach, an ATPG with sequential property that considers two full time frames is required. On the other hand, test patterns for the skewed-load ap-

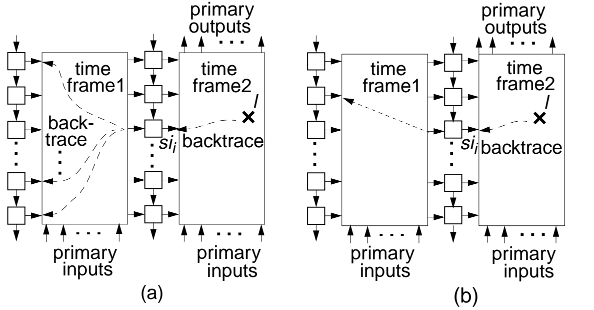

Figure 3. Assignment of State Inputs in Time Frame 2 (a) Broad-side (b) Skewed-load

proach can be generated by a combinational ATPG with little modification. Hence, longer test generation time is required for the broad-side approach.

3. Motivation and Key Idea

As described in Section 2, although the skewed-load approach has several advantages (higher fault coverage, smaller test pattern sets, and lower test generation cost) over the broad-side approach, the broad-side approach is the only choice of scan-based test method in many cases due to difficulty meeting design requirements of the skewed-load approach [12].

The cost of test application is directly determined by the size of test pattern set to be applied. Due to large test volume required to achieve satisfactory coverage, transition fault coverage is often compromised for acceptable test volume. In most compaction algorithms, don't cares in test patterns, which are not assigned binary values by the ATPG, play an important role in compacting test patterns [5, 7, 2].

Figure 3 illustrates backtrace operations during an ATPG process to generate a test pattern pair for the slow-to-rise (STR) fault at line l. Assume that state input si_i should be assigned a 1 to activate the fault and propagate the activated fault effect to primary and/or scan output(s). If we use the broad-side approach, we may need to specify a large number of state inputs in time frame 1 to set si_i to a 1 in time frame 2 (see Figure 3 (a)). On the other hand, if we use the skewed-load approach, assigning a 1 to si_i in time frame 2 is achieved by setting only si_{i-1} to a 1 in time frame 1 (see Figure 3 (b)) and no backtrace is required in time frame 1. Hence, test patterns generated by the skewed-load approach typically have more don't cares, i.e. fewer specified bits, than those generated by the broad-side approach. This implies that test patterns generated by the skewed-load approach have more room for compaction.

If only a small set of state inputs of the circuit require a large number of inputs to be specified in time frame 1 to be set to binary values in time frame 2, then controlling only

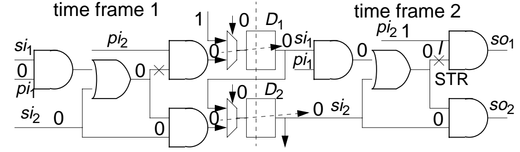

Figure 4. Dependency Untestable Fault

those state inputs by the skewed-load approach and controlling the rest of state inputs by the broad-side approach will generate test patterns that have many don't cares. Since we drive only the small set of scan flip-flops by a separate scan enable signal, the separate scan enable signal can switch in a full system clock cycle without being driven by a strong buffer or a buffer tree. The scan enable signal that drives the rest of scan flip-flops need not switch at-speed. In consequence, by using our hybrid approach, we can take advantages of the skewed-load approach without having to meet costly design requirement of the traditional skewed-load approach. In the rest of this paper, scan flip-flops that are controlled by the skewed-load (broad-side) approach are referred to as *skewed-load (broad-side) flip-flops*.

Another advantage of the hybrid approach is that some faults that are not testable by the traditional broad-side approach due to function dependency can become testable by the hybrid approach. For example, consider the STR fault at line l in the circuit shown in Figure 4. In order to initialize the STR fault, line l should be set to a 0 in time frame 1. Assume that when the select input of multiplexer of a scan flip-flop, which selects between the scan input and the normal data input, is set to a 0, the normal data input of the multiplexer is selected, i.e., the scan flip-flop is configured into its normal mode. Therefore, the 0 at line l in time frame 1 propagates to state input si_1 in time frame 2 through the AND gate and in turn sets line l to a 0 at the next cycle. However, in order to activate the STR fault in time frame 2, line l should be set to a 1. Hence, the STR fault is not testable by the broad-side approach. Now, assume that scan flip-flop D_1 is a skewed-load scan flip-flop, i.e., the select input of multiplexer of D_1 is set to a 1 to select the scan input. If the scan input is assigned a 1, then the 1 at the scan input propagates to input si_1 in time frame 2 rather than the 0 at the normal data input. If both primary inputs pi_1 and pi_2 are assigned 1's in time frame 2, the STR fault at line l can be detected at scan output so_1.

Finally, the proposed approach can speed up ATPG processes. Let us revisit Figure 3. If PODEM [4] algorithm is used to generate test patterns, setting si_i to a 1 in time frame 2 by the broad-side approach will be achieved by a series of backtrace operations in time frame 1. Whether setting si_i to a 1 in time frame 2 leads to a solution to generate a test pattern pair for the target fault at line l cannot be determined

```
Selecting skewed-load scan flip-flops
compute C1(l) and C0(l) for every line l in the circuit;
for every state output so_i;
    cost(so_i) = max(C1(so_i), C0(so_i));
for every state input si_i;
    compute shift dependency relation with si_{i-1};
sort state outputs so_i by cost(so_i) in non-increasing order
for j = 1, i = 1 to n { /* n is the number of state inputs in the circuit */
    if si_i is indepdent of si_{i-1}, then select D_i as a skewed-load flip-flop;
    increment j by 1;
    if (j > M), then exit the for loop; }
```

Figure 5. Flip-flop Selection Algorithm

until state si_i is assigned a 1 in time frame 2. If setting si_i to a 1 in time frame 2 does not lead to a solution, it is found only after a lot of CPU time has already been spent on backtrace operations and following forward implications. On the other hand, if the skewed-load approach is used, setting state input si_i to a 1 in time frame 2 requires no backtrace operations in time frame 1. If setting state input si_i to a 1 in time frame 2 does not lead to a solution, then the ATPG can immediately backtrack without wasting time on a large number of backtrace operations and following forward implications.

4. Selecting Skewed-load Flip-flops

We use controllability measures, which are similar to SCOAP [6], as the criterion to select scan flip-flops to be controlled by the skewed-load approach. We select M state outputs, where M is determined from the number of flip-flops the scan enable signal can drive without a strong buffer or buffer tree, that have highest 0 or 1 controllability measure and control the scan flip-flops that drive the selected M scan outputs by the skewed-load approach. The 0 (1) controllability measure of line l, $C_0(l)$ ($C_1(l)$), is the minimum number of primary and state inputs to be specified to set line l to a 0 (1). Controllability measures of line l are defined as:

$$C_v(l) = \begin{cases} 1 & \text{if } l \text{ is a primary or state input} \\ \min_{l_a}\{C_c(l_a)\} & \text{if } v = c \oplus i \\ \sum_{l_a} C_{\bar{c}}(l_a) & \text{otherwise,} \end{cases} \quad (1)$$

where $v \in \{0, 1\}$ and l_a and l are respectively inputs and outputs of a gate with controlling value c and inversion i. If a value c, when applied to an input of a gate, determines the value at the output of the gate regardless of the values applied to its other inputs, then the value is said to be the *controlling value* of the gate. Note that the controllability measures are calculated on one time frame version of the circuit.

If we select skewed-load flip-flops considering only controllability measures of corresponding state outputs, then it may introduce shift dependency untestable faults [9]. If a scan flip-flop drives a fanout cone that its immediate predecessor scan flip-flop also drives, then controlling the scan flip-flop by the skewed-load approach may introduce shift dependency untestable faults (see Section 2). Hence, when we select skewed-load flip-flops, we should also consider shift dependency relation between adjacent scan flip-flops to avoid introducing shift dependency untestable faults.

If state input si_i drives no fanout cones that its immediate predecessor state input si_{i-1} drives, then si_i is said to be *independent* and controlling such state inputs si_i by the skewed-load approach does not introduce any shift dependency untestable faults [9]. When we use the skewed-load approach for all scan flip-flops in the circuit, it is enough to consider only one time frame to identify independent state inputs. However, in the hybrid approach, some of scan flip-flops are controlled by the broad-side approach. Hence, in order to guarantee no decrease in fault coverage due to introduction of shift dependency untestable faults, we have to consider two time frames to identify independent state inputs. Nevertheless, according to our extensive experiments, decrease in fault coverage due to selecting state inputs that are independent in one time frame but not independent in two time frames to be controlled by the skewed-load approach is negligible. Figure 5 shows a pseudo-code for the algorithm to select skewed-load scan flip-flops.

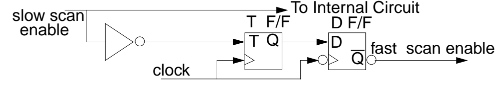

Figure 6. Fast Scan Enable Signal Generator

5. Generating Fast Scan Enable Signal

The *fast scan enable signal*, which drives skewed-load flip-flops, is internally generated from the *slow scan enable signal*, which drives broad-side flip-flops, and the system clock signal. Hence, no additional external pin is required for the fast scan enable signal. Figure 6 shows a schematic for the fast scan enable signal generator. The fast scan enable signal generator can be implemented with very little hardware. Since the fast scan enable signal is synchronized to the system clock, which is accessible from the clock pin of any flip-flop, the fast scan enable signal generator can be located anywhere in the chip to minimize routing and possible skew of the fast scan enable signal. Furthermore, since the fast scan enable signal is synchronized, it is also possible to use multiple fast scan enable signal generators, each of which drives different sets of skewed flip-flops. When there are many state outputs that have high controllability measures and hence all the scan flip-flops that have high controllability measures cannot be driven by a single fast scan enable signal without a strong buffer, then using multiple fast scan enable signals can reduce load capacitance of

fast scan enable signals by making each fast scan enable signal drive only a small set of skewed-load scan flip-flops.

6. Experimental Results

Table 6 shows experimental results for full scan versions of ISCAS 89 benchmark circuits. The experiments were conducted on a SUN Microsystem's Ultra 1 with 1 Giga bytes of memory. Results obtained by using the skewed-load, the broad-side, and the hybrid approach are compared for transition delay fault coverage (columns *% FC*), numbers of test patterns generated (columns *# Vec.*), and ATPG run time (columns *time*). We used only one fast scan enable signal in every benchmark circuit and used M (the maximum number of skewed-load flip-flops) as 10% of total number of scan flip-flops in the circuit. However, only 1 or 2 flip-flops are selected as skewed-load flip-flops (column *# SFFs*) for many circuits since those circuits have very small numbers of independent inputs.

For all benchmark circuits, except for s1196 and s1238, fault coverage achieved by test pattern sets generated by our hybrid approach is higher than that achieved by test pattern sets generated by the broad-side approach. For example, for s13207, the broad-side approach achieves only 77.74% while the hybrid approach achieves as high as 89.52%. The average fault coverage improvement over all the ISCAS89 benchmark circuits is 4.47%, with the highest improvement of 13.94%. It is notable that the hybrid approach test pattern sets achieve higher fault coverage than the skewed-load approach test pattern sets for s510, s820, s832, and s13207 for which the broad-side approach test pattern sets achieve significantly lower fault coverage. This implies that when carefully designed, the hybrid approach can achieve even higher fault coverage than the skewed-load approach, which requires very high hardware overhead.

For some circuits, the hybrid approach test pattern sets are larger than the broad-side approach test pattern sets. However, for those circuits, the hybrid approach test pattern sets achieve substantially higher fault coverage. For most circuits for which the hybrid and broad-side approaches achieve similar fault coverage, hybrid approach test pattern sets are smaller than broad-side test pattern sets. The only exception is s38417 for which the hybrid approach attains similar fault coverage to broad-side approach while the hybrid test pattern set for s38417 has about 100 more patterns than the broad-side test pattern set. This is due to inaccuracy in controllability measures used as the criterion to select skewed-load flip-flops. Note that the 1 (0) controllability measure at a line reflects the minimum number of inputs to be specified to set the line to a 1 (0). However, due to conflict with other required assignments during the test generation process, setting a line to a binary value by specifying only minimum number of inputs is often not possible. If state output so_i has a very high 1 controllability measure $C_1(so_i)$ but very low 0 controllability measure $C_0(so_i)$, then the corresponding scan flip-flop D_i will likely be selected as a skewed-load flip-flop since the cost of so_i, $cost(so_i) = max\{C_0(so_i), C_1(so_i)\}$, is very high (see Figure 5). However, if so_i is required to be assigned 0's in most test patterns, selecting scan flip-flop D_i as the skewed-load flip-flop will not help generate compact test pattern sets. A new cost function that can correct above limitations of the current cost function is under investigation.

The ATPG run time of the hybrid approach is comparable to that of the broad-side approach for most circuits except a few circuits such as s13207, s5378 and s38417. For s13207, the ATPG run time of the hybrid approach is substantially shorter than that of the broad-side approach while the ATPG run time of the hybrid approach is substantially longer than that of the broad-side approach for s5378 and s38417.

7. Conclusions

In this paper, a novel scan-based delay test approach, referred as the hybrid delay scan, has been proposed. The proposed method combines advantages of skewed-load and broad-side approaches and can achieve higher delay fault coverage than the broad-side approach. By selecting only a small fraction of the state inputs as the skewed-load flip-flops, we avoid the costly design requirement of the skewed-load approach due to the fast scan enable signal that must switch in a full system clock cycle.

Our experimental results show that for all ISCAS 89 benchmark circuits, the transition delay fault coverage achieved by the hybrid approach is higher than or equal to that achieved by the broadside load approach, with an average improvement of 4.5%. Due to limitation of the current cost function used as the criterion to select skewed-load flip-flops, reduction in test set sizes is not spectacular. A new cost function that improves the current cost function is under investigation.

Some circuits have very small numbers of independent state inputs. If such circuits have large numbers of state inputs with high controllability measures, then reduction in test pattern set sizes and enhancement of fault coverage that are obtained by using the hybrid approach may not be significant. If we use multiple fast scan enable signals, then we can obtain large reduction in test set sizes and improvement in fault coverage even for such circuits. If we partition an entire test application task into several sub-phases and control a different subset of scan flop-flops by fast scan enable signals at each sub-phase, then faults that are not detected due to shift dependency in a sub-phase can be detected in other sub-phases. We are currently investigating algorithms to partition skewed-load flip-flops into several subsets to further enhance fault coverage and reduce test set sizes.

Table 1: Experimental Results

CKT		*Skewed-load*			*Broad-side*			*Hybrid*			
Name	*# FFs*	*% FC*	*# Vec.*	*time*	*% FC*	*# Vec.*	*time*	*# SFFs*	*% FC*	*# Vec.*	*time*
s208	8	83.43	41	0.13s	69.23	28	0.29s	1	73.96	33	0.13s
s298	14	78.79	30	0.13s	79.17	30	0.39s	2	87.12	48	0.22s
s344	15	92.13	37	0.15s	92.88	36	0.35s	1	96.63	46	0.18s
s349	15	92.31	38	0.15s	93.04	42	0.42s	1	96.70	48	0.14s
s386	6	88.44	76	0.25s	66.33	47	0.89s	1	80.27	63	0.72s
s420	16	82.35	80	0.59s	68.24	53	1.32s	1	70.00	56	0.60s
s444	21	87.70	38	0.22s	77.01	42	1.32s	3	79.14	47	1.26s
s510	6	86.85	80	0.60s	84.13	79	2.26s	1	93.88	88	1.25s
s526	21	83.30	70	0.46s	60.89	58	2.11s	3	68.92	70	2.05s
s641	19	99.49	57	0.60s	95.67	83	9.33s	2	96.44	78	16.46s
s713	19	99.56	66	0.79s	94.32	91	17.20s	2	94.98	76	38.11s
s820	5	84.62	131	1.67s	77.49	133	10.46s	1	85.04	138	21.05s
s832	5	84.52	141	1.70s	77.13	135	11.43s	1	84.94	148	21.89s
s838	32	81.71	152	3.08s	67.55	104	6.73s	1	68.44	108	2.93s
s953	29	91.94	133	2.30s	92.43	134	6.49s	3	95.85	135	6.36s
s1196	18	99.91	227	4.72s	99.81	237	8.06s	2	99.81	217	2.36s
s1238	36	99.91	232	7.58s	99.72	233	12.10s	2	99.72	231	5.61s
s1423	74	95.41	113	12.44s	87.73	134	9m23s	8	88.48	129	14m7s
s1488	6	76.22	145	4.31s	85.59	151	24.13s	1	91.80	171	21.8s
s1494	6	75.88	145	4.25s	85.51	147	24.00s	1	91.81	170	22.45s
s5378	179	92.22	336	47.34s	93.02	365	9m2s	18	94.76	349	22m40s
s9234	228	91.89	605	12m50s	83.01	643	83m21s	23	84.98	598	126m27s
s13207	669	88.27	654	8m48s	77.74	620	24m48s	67	89.52	803	17m5s
s15850	597	92.53	595	22m6s	66.17	508	113m16s	60	72.56	524	166m1s
s35932	1728	100.0	125	7m11s	93.80	131	11m58s	173	99.58	175	6m40s
s38417	1636	98.57	1705	136m26s	96.80	1566	226m23s	164	96.84	1669	505m33s
s38584	1452	92.48	1097	82m15s	90.21	1463	759m47s	146	93.20	1528	898m31s

References

[1] D. Belete, A. Razdan, W. Schwarz, R. Raina, C. Hawkins, and J. Morehead. Use of DFT Techniques In Speed Grading a 1GHz+ Microprocessor. In *Proceedings IEEE International Test Conference*, pages 1111–1119, 2002.

[2] J.-S. Chang and C.-S. Lin. Test Set Compaction for Combinational Circuits. *IEEE Trans. on Computer-Aided Design of Integrated Circuit and System*, Vol. 14(11):1370–1378, November 1995.

[3] S. Comen. DFT-focused chip testers: What can they really do? In *Proceedings IEEE International Test Conference*, page 1120, 2000.

[4] P. Goel. An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits. *IEEE Trans. on Computers*, Vol. C-30(3), Mar. 1981.

[5] P. Goel and B. C. Rosales. Test Generation & Dynamic Compaction of Tests. In *Dig. Papers Test Conference*, pages 182–192, 1979.

[6] L. H. Goldstein and E. L. Thigpen. SCOAP: Sandia Controllability/Observability Analysis Program. In *Proceedings IEEE-ACM Design Automation Conference*, pages 190–196, 1980.

[7] I. Pomeranz, L. N. Reddy, and S. M. Reddy. COMPACTEST: A Method to Generate Compact Test Sets for Combinational Circuits. In *Proceedings IEEE International Test Conference*, pages 194–203, 1991.

[8] G. D. Robinson. DFT-focused chip testers: What can they really do? In *Proceedings IEEE International Test Conference*, page 1119, 2000.

[9] J. Savir. Skewed-Load Transition Test: Part I, Calculus. In *Proceedings IEEE International Test Conference*, pages 705–713, 1992.

[10] J. Savir and S. Patil. Scan-Based Transition Test. *IEEE Trans. on Computer-Aided Design of Integrated Circuit and System*, Vol. 12(8), August 1993.

[11] J. Savir and S. Patil. Broad-Side Delay Test. *IEEE Trans. on Computer-Aided Design of Integrated Circuit and System*, Vol. 13(8), August 1994.

[12] J. Saxena, K. M. Butler, J. Gatt, R. R, S. P. Kumar, S. Basu, D. J. Campbell, and J. Berech. Scan-Based Transition Fault Testing - Implementation and Low Cost Test Challenges. In *Proceedings IEEE International Test Conference*, pages 1120–1129, 2002.

[13] J. A. Waicukauski, E. Lindbloom, B. K. Rosen, and V. S. Iyengar. Transition Fault Simulation. *IEEE Design & Test of Computers*, pages 32–38, April 1987.