ULSI Interconnect Length Distribution Model Considering Core Utilization

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Abstract

Interconnect Length Distribution (ILD) represents a correlation between the number of interconnects and length. The ILD can predict power consumption, clock frequency, chip size, etc. It has been said that high core utilization and small circuit area improve chip performance. We propose a ILD model to predict a correlation between core utilization and chip performance. The proposed model predicts influences of interconnect length and interconnect density on circuit performances. As core utilization increases, small and simple circuits improve the performances. In large complex circuits, decrease of load capacitance is more important than that of total interconnect length for improvement of chip performance. The proposed ILD model expresses actual ILD more accurate than conventional models.

1. Introduction

In recent technologies, the circuit performance of ULSI greatly depends on the delay and power consumption of interconnects. The analysis of interconnects is important for the evaluation and prediction of chip performance. The interconnect length distribution (ILD) of circuits can evaluate chip performance of a new architecture like X architecture and 3D-SoC, and predict some problems like the cross-talk, *etc.* [1-4].

It has been said that high core utilization and small circuit area improve chip performance. This paper examines influences of core utilization on circuit performances. The conventional ILD model assumes that gates are arranged uniformly in the whole circuit area as shown in Fig.1(A). In actual layouts of cell-base design, gates are placed in the row of the fixed height and each cell size is different as shown in Fig.1(B). We propose a ILD model considering core utilization. The proposed model evaluates influences of interconnect length and interconnect density on circuit performances.

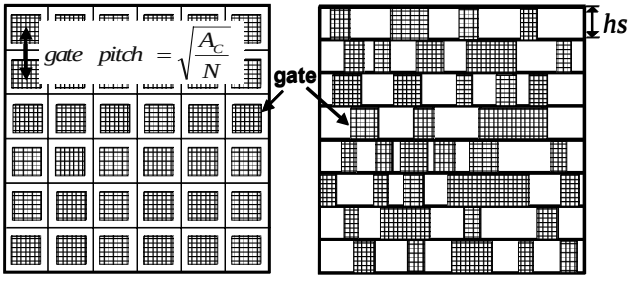

Fig. 1 Gate placing of conventional model and actual layouts of cell-base design.

In this paper, we explain a method to extract ILD parameters at first. It contributes to accurate prediction of LSI performance. Second, we propose a new ILD model to consider core utilization. The model characterizes actual cell-based layouts like Fig.1(B). Finally, we demonstrate simulated results, which are correlations between core utilization and chip performance. We show a guideline of ULSI design considering core utilization.

2. Extracting the ILD Parameters

In order to clarify a correlation between core utilization and chip performance, we propose a new ILD considering core utilization. This section explains how to extract ILD parameters from P&R (Place and Routing) summary, and an accurate extraction is important to predict chip performance.

Figure 2 summarizes the conventional analytical expression of ILD, where $i(\ell)$ is the number of interconnects of length ℓ, and ℓ is interconnect length in units of gates pitch. This expression is derived based on Rent's empirical law [5][6]. The correlation between the number of pins $\boldsymbol{T}$ and the number of gates $\boldsymbol{N}$ is given by

$$T = kN^{p_T} \tag{1}$$

where $\boldsymbol{k}$ and $\boldsymbol{p_T}$ are Rent's constants, representing the ave-

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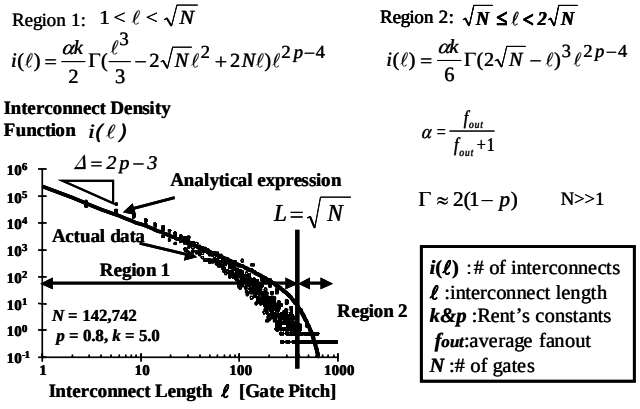


Fig. 2 Conventional analytical ILD expression. Data are from Ref. [5].

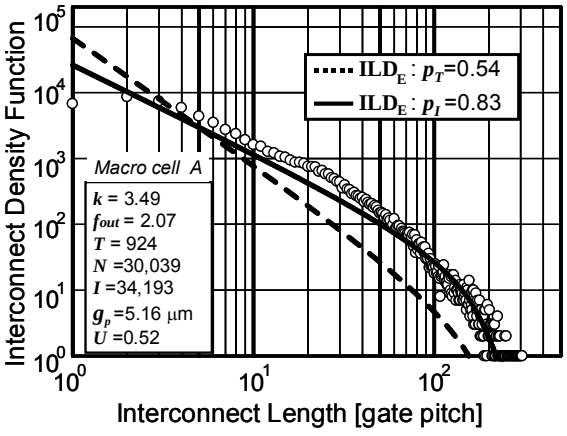


Fig.3 ILD_R from wiring data of Synopsys Apollo P&R data of a macro cell of a commercially available 0.13μm chip.

rage number of ports and a constant related to the complexity of the circuit, respectively. Usually, complex circuits tend to have large p and small k, while simple circuits tend to have small p and large k [6].

In the conventional ILD expression curve, the slope at small gate pitch equals to $2p$-3 as shown in Fig.2 [7]. We have confirmed that the gate pitch (g_p) should be defined by

$$g_p = \sqrt{\frac{A_C}{N}} \tag{2}$$

where A_C is the circuit area [1]. ILD_R is actual wire length distribution extracted from layout. Since the analytical expression of ILD is a function of gate pitch, ILD_R should be depicted as a function of gate pitch. Figure 3 shows the correlation between ILD_R and ILD_E. Here, the analytical ILD expression is called as ILD_E. The circles indicate ILD_R, which is the number of interconnect integrated at every gate pitch. The ILD parameters are extracted from P&R summary. In the P&R summary, the following parameters are listed: circuit area (A_C), number of gates (N), total number of interconnects (I), average fanout (f_{out}) and average pin number of gate (k). We propose two methods of Rent's constant p extraction. The first method is that Rent's constant p_T is derived from the Eq.(1), and the another method is that Rent's constant p_I is derived from

$$I = \frac{f_{out}}{f_{out}+1} k(N - N^{p_I}) \tag{3}$$

where I is the total number of interconnects. Eq.(3) is derived from the total number of interconnects [8]. In Fig.3, dotted ILD_E curve is plotted using k and p_T from Eq.(1). Solid ILD_E curve is plotted using p_I value which is determined by Eq.(3) using the parameters listed in P&R summary. As shown in Fig.3, the dotted curve does not fit ILD_R in the all region. On the other hand, the solid curve fits ILD_R except the short interconnect length region.

3. New Analytical ILD Expression Considering Core Utilization

The conventional ILD model does not consider core utilization. We propose a new analytical ILD expression. The proposed ILD model considers core utilization (U) as shown in Fig. 4. Here core utilization (U) is

$$U = \frac{cell\ \ area}{circuit\ \ area} \ . \tag{4}$$

In the conventional model Fig.1 (A), the model is assumed that all cell has a constant area, these are arranged uniformly in the whole circuit area, the shape of cells is a square, and the position of all terminal is center in a cell. In actual layout Fig.1 (B), the width of cell, the position of terminals, and core utilization are not constant. The distance from the cell to the adjacent cell is varied. The core utilization is usually described in P&R summary. The core utilization, the cell sizes and the position of terminal are modeled as shown in Fig. 4. The solid line shows an interconnect between the center cell and four adjacent cells. Space area is determined by core utilization, and cells are arrayed in space area. In the new model, a pin is arranged anywhere in a cell area. The cell width, a and b_ℓ (ℓ=1, 2, 3, 4) in Fig. 4, are assumed to be uniformly distributed from W to $4W$. Note that W is minimum standard cell width. A probably distribution of interconnect length is calculated by Monte Carlo simulation as shown in Fig.5. Probability distribution becomes gentle and the peak transfers to long interconnect length as the core utilization decreases. In the conventional analytical ILD expression, the interconnect length is a discrete value in unit of gate pitch [5], because the conventional ILD model assumes that the gates are arranged uniformly.

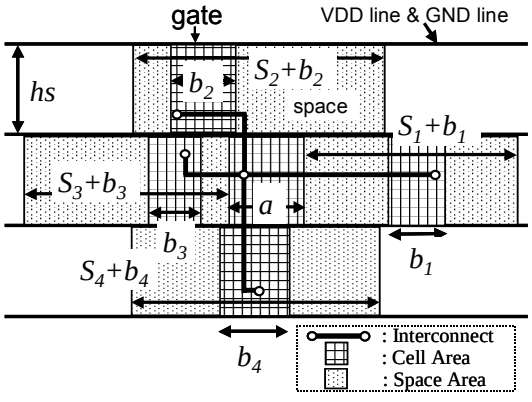


Fig.4 The proposed model.

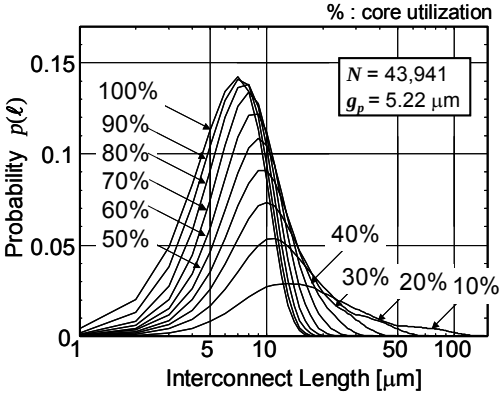


Fig.5 Wire length distribution among adjacent gates based on the model Fig. 4.

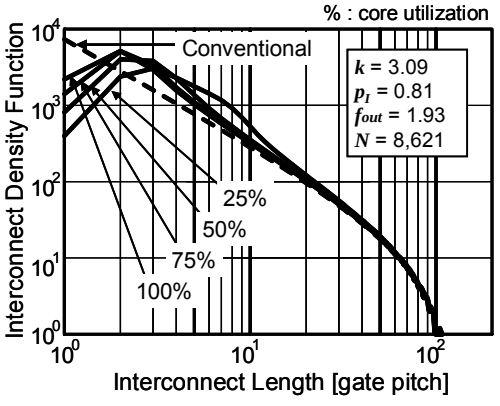


Fig.6 ILD considering core utilization (U).

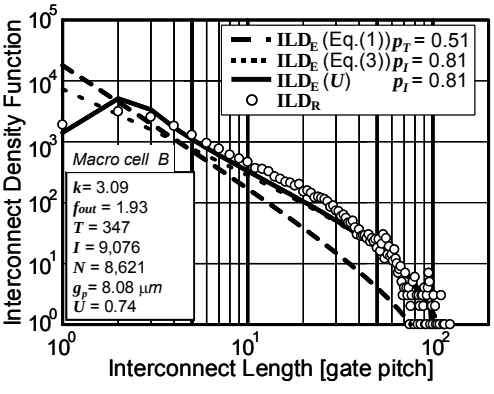


Fig.7 ILD from wiring data of Synopsys Apollo P&R data of a macro cell of a commercially available 0.18μm chip.

A probability distribution in Fig. 5 can represent ILD expression as continuous equation. $P(t)$ is probability with interconnect length from t-1 to t. The probability of interconnect length in unit of gate pitch $P(t)$ is derived from the probability distribution in Fig.5, and $P(t)$ is derived by

$$P(t) = \int_{(t-1)\cdot gp}^{(t)\cdot gp} p(\ell)d\ell \tag{5}$$

where ℓ is interconnect length. Assuming $P(t)$ can be applied to each gate pitch, $i'(t)$ is obtained by

$$i'(t) = \sum_{m=1}^{t} P(m)i(t-m+1) \tag{6}$$

where $i'(t)$ is the proposed $\mathbf{ILD_E}$ in consideration of core utilization. Figure 6 shows ILD with various core utilizations. Dashed lines are calculated by the conventional model. Solid line is calculated by the proposed model. When the core utilization is decreased, the number of interconnects decreases at short interconnect length region. Figure 7 shows $\mathbf{ILD_R}$ extracted from layout data and $\mathbf{ILD_E}$ calculated from P&R summary parameters of $\boldsymbol{p}$, $\boldsymbol{f_{out}}$, $\boldsymbol{k}$, $\boldsymbol{N}$ and $\boldsymbol{U}$. Dashed line is calculated using $\boldsymbol{p}_T$ (Eq.(1)). Dotted line is calculated using $\boldsymbol{p}_I$ (Eq.(3)) and P&R summary. Solid line is ILD with the core utilization ($\boldsymbol{U}$) that is listed in P&R summary. It is noted that the solid $\mathbf{ILD_E}$ curve represents the $\mathbf{ILD_R}$ of wiring data in whole gate pitch region.

4. Evaluation of Power Consumption and Frequency

ILD can estimate the several circuit performances. The conventional ILD cannot estimate the performance in consideration of core utilization. The proposed $\mathbf{ILD_E}$ predicts a correlation between core utilization and chip performance. High core utilization and small circuit area are generally said to improve chip performance. This paper examines how much performance changes by the core utilization. In order to calculate the power consumption and frequency, the load capacitance per unit of interconnect C_{int} should be calculated. In this paper, we assume 0.18 μm CMOS technology. We use a calculating method of C_{int} in

Ref. [1]. Figure 8 shows the model of C_{int}, and the thickness of all layers is constant. This simulation uses the parameters of Fig.8. The distance S in Fig.8 is calculated by

$$S=\frac{A_C \cdot n}{L_{total}}-W \tag{7}$$

where A_C is circuit area, L_{total} is total interconnect length, W is line width and n is number of interconnect layers. Total load capacitance C_{total} and the load capacitance per unit length C_{int} are calculated as follows [1].

$$C_{total}=C_{int}\sum_{\ell=1}^{2\sqrt{N}}\ell\cdot i(\ell)=C_{int}L_{total} \tag{8}$$

$$C_{int}=2C_{ground}+2C_{line-to-line}$$

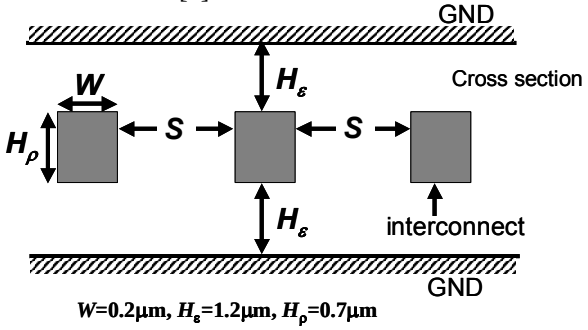
$$\frac{C_{ground}}{\varepsilon}=\frac{W}{H_\varepsilon}+1.086\begin{pmatrix}1+0.685e^{-(H_\rho/1.343S)}\\-0.9964e^{-(S/1.421H_\varepsilon)}\end{pmatrix}\cdot\left(\frac{S}{S+2H_\varepsilon}\right)^{0.0476}\left(\frac{H_\rho}{H_\varepsilon}\right)^{0.337} \tag{9}$$

$$\frac{C_{line-to-line}}{\varepsilon}=\left(\frac{H_\rho}{S}\right)\begin{pmatrix}1-1.897e^{-(H_\varepsilon/0.31S)-(-H_\rho/2.474S)}\\+1.302e^{-H_\varepsilon/0.082S}\\-0.1292e^{-H_\rho/1.326S}\end{pmatrix}+1.722\left(1-0.6548e^{-W/0.3477H_\varepsilon}\right)e^{-S/0.651H_\varepsilon} \tag{10}$$

The power consumption is calculated as follows [5].

$$P=\frac{1}{2}a\cdot C_{total}\cdot f_C\cdot V_{dd}^2 \tag{11}$$

where a is the average activity factor, V_{dd} is the supply voltage, f_c is clock frequency, C_{total} is the total load capacitance, C_{int} is load capacitance per unit length and L_{total} is total interconnect length. Frequency and V_{dd} are assumed to be 133MHz and 1.8V, respectively. The frequency is calculated as follows [9].



W=0.2μm, H_ε=1.2μm, H_ρ=0.7μm

# of interconnect layers:5

Dielectric constant(SiO_2):3.9

Fig.8 Cross-section of interconnect model (typical 0.18μm technology).

$$f_C=\frac{1}{T_C}=\frac{1}{n_{ld}\cdot T_g+T_{skew}} \quad . \tag{12}$$

where n_{ld} is logic depth and T_{skew} is clock skew time. T_g is a gate delay. T_g is calculated by

$$T_g=R_{gout}f_{out}(0.86\cdot C_{int}\ell_{av}+0.86\cdot C_{gin})+R_{int}\ell_{av}(0.37\cdot C_{int}\ell_{av}+0.86\cdot C_{gin}) \tag{13}$$

where ℓ_{av} is average interconnect length, R_{gout} is gate output resistance, C_{gin} is gate input capacitance and R_{int} is interconnect resistance per unit length. Substituting Eq.(12) into Eq.(13), f_c is given by

$$f_C=\frac{1}{n_{ld}\left[\begin{matrix}R_{gout}f_{out}(0.86\cdot C_{int}\ell_{av}+0.86\cdot C_{gin})\\+R_{int}\ell_{av}(0.37\cdot C_{int}\ell_{av}+0.86\cdot C_{gin})\end{matrix}\right]} \tag{14}$$

where clock skew time T_{skew} is ignored.

Figure 9 shows the correlation between total interconnect length and load capacitance per unit length and the core utilization for the complex circuits (***p***=0.8, ***k***=3, f_{out}=2) and simple circuits (***p***=0.2, ***k***=5, f_{out}=4), which the number of gates is different. We assume that: when the core utilization is 1.0, the circuit area is $A_C=2\times10^5$ μm^2 at ***N***=10K, $A_C=2\times10^6$ μm^2 at ***N***=100K, $A_C=2\times10^7$ μm^2 at ***N***=1M. The load capacitance per unit length of simple circuit has the minimum value in the region of core utilization 0.2 - 0.3. In the small complex circuits, the load capacitance per unit length decreases as the core utilization increase. In the large complex circuit, the load capacitance per unit length increases as the core utilization increases. This trend depends on the technology.

The frequency and power consumption are evaluated by the result and Eq.(8-14). Table 1 represents the parameters for this simulation. Active factor a and logic depth n_{ld} are based on Ref[10] and Ref[6], respectively. Figure 10(a) shows correlations between frequency and the core utilization in the complex and simple circuits. As the core utilization increases, the difference of frequency between complex and simple circuits increases. On the other hand, the frequency in complex circuit, which has 1M gates, decreases.

Power consumption	
Frequency f_c	133 [MHz]
Supply voltage V_{dd}	1.8 [V]
Average activity factor a	0.1
Frequency	
Gate output resistance R_{out}	8K [Ω]
Gate input capacitance C_{gin}	2 [fF]
Logic depth n_{ld}	20
interconnect resistance per unit length R_{int} (Al)	0.6 [Ω/μm]

Table 1. Parameters for prediction of power consumption and frequency

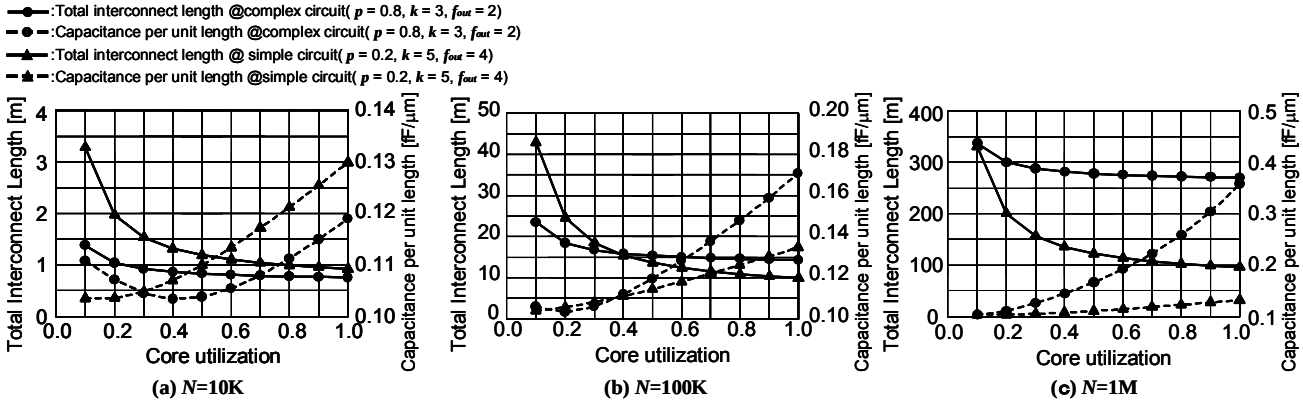


Fig.9 Total interconnect length and capacitance per unit length as a function of core utilization.

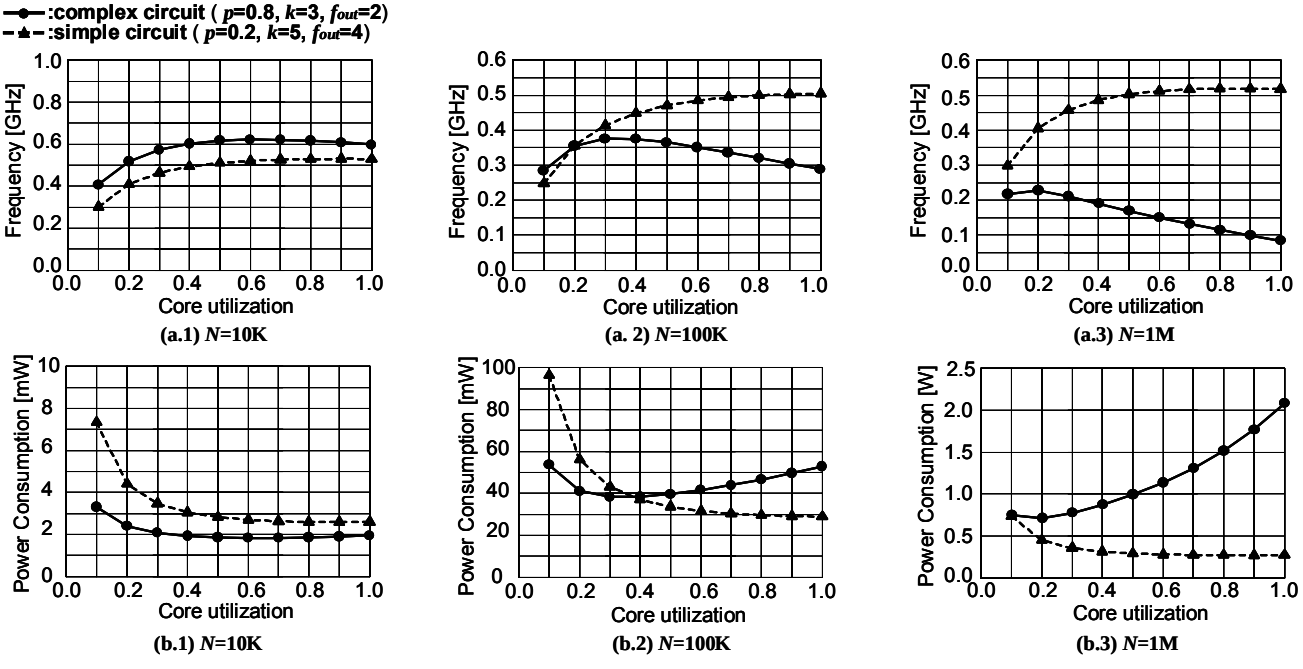


Fig.10 Frequency and power consumption as a function of core utilization.

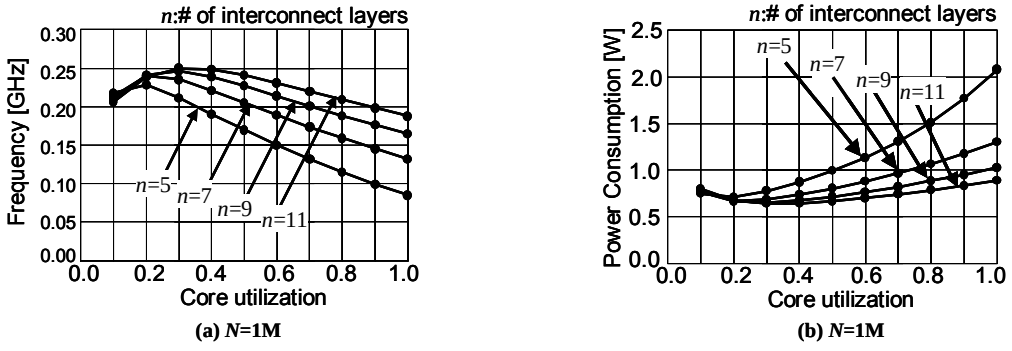


Fig.11 Frequency and power consumption in various numbers of layers as a function of core utilization.

Figure 10(b) shows correlations between power consumption and the core utilization in the complex and simple circuits. The power consumptions of 10K-gates circuits become almost constant when the core utilization is > 50%. As the core utilization increases, the power consumption of 100K-gates and 1M-gates complex circuits increases. This effect caused by the rapid increase of C_{int} in region of high core utilization. When the parameters in Table 1 change, these curves of power consumption and frequency move in parallel. It is generally said that high utilization and small circuit area improve chip performance. When the number of gates exceeds 100K, the decrease of load capacitance is more important than that of total interconnect length to improve chip performance.

In order to improve chip performance, core utilization should be not too large in complex large circuit as shown in Fig.10. Figure 11 shows a correlation between core utilization and chip performance in various numbers of layers. The maximum point of frequency and the minimum point of power consumption hardly move as shown in Fig.11. Frequency and Power consumption are improved as the number of layers increases. In the large complex circuit, decreasing core utilization is more important than increasing the number of layers. In the future, the number of gates in a LSI will increase [11], so this new ILD considering core utilization will be important in future LSI designs.

5. Conclusion

The ILD can predict chip performance. In order to predict a correlation between core utilization and chip performance, we propose a ILD model which considers core utilization. The proposed model predicts the influence of interconnect length and interconnect density on circuit performance. As core utilization increases, small and simple circuits improve the performance. In large complex circuits, decrease of load capacitance is more important than that of total interconnect length for improvement of chip performance. We show a guideline of ULSI design considering core utilization.

Acknowledgements

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