Status of IEEE Testability Standards 1149.4, 1532 and 1149.6

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Introduction

Ben Bennetts, *Bennetts Associates*

Abstract

Single board, and now multi-board testability is highly conditioned by the availability of various forms of boundary scan technology. This paper surveys the three more recent IEEE Standards relating to boundary scan. The paper is based on three backgrounders prepared by members of the individual Working Groups for the IEEE Standards booth at ITC 2003.

IEEE 1149.4-1999 Mixed-Signal Test Bus Standard

The question of "What to do with analog pins on mixed-signal devices?" was not addressed by the IEEE 1149.1 Boundary Scan Standard. The question was acknowledged but put on one side by JTAG but was subsequently addressed by the publication of the 1149.4 Standard, nine years later. 1149.4 builds on 1149.1 i.e. is a superset of 1149.1, and makes provision for very special boundary scan cells, called Analog Boundary Modules (ABMs) on the analog pins. The ABMs are capable of driving and receiving both digital and analog stimulus and response.

Analog stimulus signals (DC or AC) are driven into the device on a special analog test input called Analog Test 1 (AT1) and the analog response is observed at another special analog test output, AT2. Distribution of the analog stimulus and response is achieved via two internal analog busses, AB1 and AB2. Each ABM is a collection of programmable switches (conceptually) that can be programmed to set up an ABM as an analog or digital driver, or an analog or digital sensor.

Adoption of the 1149.4 Standard has been slow so far, possibly because analog designers are not aware of the 1149.4 solution or, if they are aware, because they are concerned about the potential impact on performance once the ABMs are inserted. There may also be a perception that ABMs are expensive to design and build but this is a matter of DFT economics i.e. what is the gain versus what is the pain? Also, only one EDA test-synthesis vendor is currently supporting an 1149.4 design flow. But, 1149.4 is certainly alive and well in the university research domains, generally sponsored by industry (telecommunications, automotive), and National Semiconductor announced in 2002 the availability of an 1149.4 demonstrator device, the STA400 analog multiplexer/demultiplexer device.

IEEE 1532-2002 In-System Configuration of Programmable Devices Standard

Several years ago, there was a move in the board design community to start programming devices such as complex programmable logic devices (CPLDs) and field-programmable gate arrays (FPGAs) on the board. In-system programming, as it became known, had distinct advantages over off-board programming on an off-line programming station. For example, there was no need to insert and remove the device for re-programming, ability to re-program throughout the life cycle of the product, a reduction of pre-programmed spare parts, etc. It was not long before board designers began asking the PLD vendors to provide a programming path through the existing 1149.1 boundary-scan chains on the board and the result was a collaborative effort between the two industries of PLD vendors and boundary-scan board tester vendors, resulting in the 1532 In-System Configuration (ISC) Standard in 2000.

This Standard, also a superset of the 1149.1 Boundary-Scan Standard, provides for defined data and address registers inside the PLD for programming purposes. Access to and use of these registers is through a series of special *ISC_xxx* instructions executed through the standard 1149.1 Test Access Port. The instructions allow a device to be programmed, its contents verified, its contents erased, and its contents secured: all this through the surrounding boundary-scan chain whilst the device is mounted on a board.

Additionally, the standard defines external device behaviours before, during and after programming so that system designs can ensure that these devices do no harm during the configuration operations. Similarly, the standard mandates that devices in which programming is terminated abnormally do not disturb the integrity of the system. These rules ensure that highly reliable programmable systems can be developed.

Commercial take-up of 1532 structures is now gaining momentum with several PLD vendors announcing 1532-compliant devices. Board tester vendors are also announcing support for board-level scan chains that include 1532-compliant devices. It is clear that 1532 is here to stay.

IEEE 1149.6-2003 Boundary Scan Testing of Advanced Digital Networks

Within the telecommunication industry, there has been a move to make use of low-voltage differential signalling (LVDS) to preserve noise immunity for signal transmissions down at the 3.3 V level and lower.

LVDS also allows high data rate transmissions with low power consumption and low EMI emissions. 1149.1 does not really address the problem of what to do with the two differential legs of an LVDS interconnect other than to suggest placing a boundary-scan cell upstream of the line driver and downstream of the line receiver. This clearly is inadequate for detecting certain opens and shorts on the LVDS lines. It also may be incompatible with the small signal differentials of LVDS interconnects working at GHz frequencies.

1149.4 requires ABMs on each individual LVDS line but this is perceived to be an expensive solution, possibly incurring performance penalties.

Consequently, the 1149.6 working group took a fresh look at the whole problem area of LVDS, especially the problems of AC-coupled LVDS interconnects. AC-coupling occurs when two devices using different voltage levels for logic-1 and logic-0 need to communicate with each other. Under these conditions, the DC component of the signal is filtered out with a coupling capacitor.

1149.1 does not address AC-coupled interconnects. The Standard assumes DC-coupled lines. 1149.4 does address AC-coupled interconnects (in Analog mode) but somewhat crudely. 1149.6 addresses the problem by using a digital pulse driver boundary-scan cell at the source and special receiver boundary-scan cells at the two receiver ends extracting digital information from the received AC-coupled signal. The receiver, based on a hysteretic comparator, extracts a test-signal response from an off-set signal, converting the response back into logic-1/logic-0 responses.

1149.6 has only just been approved (in 2003) but already demonstrator devices exist (from Agilent Technologies and National Semiconductor) so clearly the need is there to move this Standard into commercial use as fast as possible.

References

1. K. Parker, The Boundary Scan Handbook, 3rd Edition, Kluwer 2003
   Note: this book covers all three Standards described in this paper plus covers the main IEEE 1149.1 Boundary Scan Standard
2. R G "Ben" Bennetts, "The current state of boundary scan technology ", Evaluation Engineering Newsletter, November 2003. Available from http://www.evaluationengineering.com/newsletter/1003bs.htm

IEEE Standard 1149.4 Mixed Signal Test Bus

Steve Sunter, *LogicVision*, Adam Osseiran, *NNTTF* and Adam Cron, *Synopsys*

What is IEEE STD 1149.4?

This standard describes a set of rules, each of which is necessary and sufficient for any analog bus that has an 1149.1-compliant control infrastructure.

What is it used for?

The bus is appropriate for analog, mixed-signal, and digital parametric testing of ICs, and testing of boards containing these ICs.

How can I use it?

The standard specifies a 2- or 4-pin analog test access port (ATAP), a test bus interface circuit (TBIC), 2- or 4-wire on-chip and off-chip analog busses, and any number of analog boundary modules (ABMs). One ABM is required on-chip for each analog I/O pin (and optionally, any digital pins), each needing 4 boundary scan bits: 2 to control the output data value, tristate, and connection to AC ground, and 2 to enable access to the two analog busses.

What does it achieve?

The two busses enable simultaneous delivery of a stimulus current (or voltage) and conveying of a response voltage. The scan-controlled analog switches are typically simple CMOS transmission gates <10kohm, and if correct test techniques are used and the measured complex impedances are between 10ohm and 100 Kohm, then measurement accuracy can be better than 1%. The stimulus signals are intended to typically be <10 kHz, <100 µA, and <100 mVAC, though they may be any greater value that an IC design accommodates. Analog circuitry in ICs that include 1149.4 access to internal analog nodes can be tested more systematically, and with reusable tests. ICs that have parametric access to pins may be testable with reduced pin-count access, which may facilitate lower cost, multi-site testing. Boards that contain ICs that have 1149.4 access to pins permit measurement of passive components values that might be otherwise uneconomical or impractical to access. Such boards may be testable by ultra low cost testers, such as commonly available, or by mixed-signal data acquisition cards.

What is the status today?

A significantly increasing interest has been noticed in the last few months. Communication and medical equipment companies have already developed prototypes and are including 1149.4 in their future products. Several test chips (and a few product chips) have been fabricated with 1149.4 capabilities, but the only one that is generally available, and that is general purpose, is available in sample quantities at

http://www.national.com/appinfo/scan/

For more information

1149.4 official web-site:
http://grouper.ieee.org/groups/1149/4/index.html
Email aliases: Working Group stds-1149-4wg@mail.ieee.org
Interested people stds-esd@mail.ieee.org
To join either, follow the link on the 1149.4 web site.

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16. C Jeffrey, A Lechner, A Richardson (University of Lancaster, UK) "Online Monitoring for Automotive Subsystems Using 1149.4" Digest BTW 2003, Paper 1.3

IEEE Standard 1532 In-System Configuration of Programmable Devices

Neil Jacobson, *Xilinx* and Dave Bonnett, *ASSET-InterTech*

Description

Programmable logic radically changed the electronic system design landscape. It reduced the board space needed for random logic, state machines and system interfaces. It allowed faster design cycles, made easy late term bug fixes and gave designers greater freedom to experiment and prototype.

In-system programming of these devices has had a similar revolutionary effect. The ability to change the programmed content of programmable logic while it is on the board allows redesign of all the hardware - without changing a single component.

This allows the possibility of providing field upgrades of your product to fix problems or to introduce new functionality. It allows designing in reconfiguration as an essential function of your system with different abilities swapped in as needed during run-time. Further, it allows storage of different product profiles for retrieval as necessary to allow just-in-time configuration of systems to meet market needs.

Recent developments in programmable logic have helped in making realizing reconfigureable systems more streamlined. The most significant development, though, was the introduction, approval and popularisation of IEEE STD 1532, the IEEE Standard for In-System Configuration of Programmable Devices.

This standard approved in its final form in 2002, describes a series of mandatory and optional instructions and associated data registers that define a standard method for accessing and configuring programmable devices. The standard builds on the foundation of IEEE Std 1149.1 and requires that compliant devices first comply with IEEE Std 1149.1. It describes the behaviour of compliant devices before, during and after configuration so engineers can design safe and manufacturable programmable systems. It also extends the functionality of the BSDL (Boundary-Scan Description Language) file to include algorithmic information suitable for automating devices configuration. The standard also allows multi-vendor concurrent programming so overall system programming times can be dramatically reduced, decreasing overall manufacturing costs.

Distinct from compliant devices, the standard allows that certain devices that may not be fully compliant can have their algorithms described using the 1532 BSDL information. These devices are termed "compatible". Such devices may not offer either the safety of 1532 compliant devices nor the ability to have their programming algorithms executed concurrently with 1532 compliant devices. This presence of the keyword "proprietary" in the algorithmic description of the device in the associated BSDL file is a signal of a compatible device.

Applications

- Desktop (Socket) Programmers
- Stand-alone applications using 1149.1 TAP connections
- Automatic Test Equipment
- Embedded Systems

For more information

On the Web:
http://grouper.ieee.org/groups/1532/index.html
Email Group (restricted membership): stds-1532-wg@ieee.org
Personal Contact: Neil Jacobson – Working group chair (n.g.jacobson@ieee.org)

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17. IEEE Std 1532-2002 - IEEE Standard for In-System Configuration of Programmable Devices. IEEE Standards Association. 2002.
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IEEE Standard 1149.6 Boundary-Scan Testing of Advanced Digital Networks

Bill Eklow, *Cisco* and Carl Barnhart, *Cadence*

Description

IEEE Std. 1149.6 defines an extension to IEEE Std. 1149.1-2001 to standardize the boundary scan structures and methods required to ensure simple, robust, and minimally intrusive boundary scan testing of advanced digital networks not adequately addressed by existing standards, especially those networks that are AC-coupled, differential, or both, in parallel with IEEE Std. 1149.1 testing of conventional digital networks and in conjunction with IEEE Std. 1149.4 testing of conventional analog networks. This standard is complementary to IEEE 1149.4, specifically targeting parallel testing of advanced digital networks while IEEE1149.4 focuses on serial testing of more traditional analog networks. The standard also specifies the software and BSDL extensions to IEEE Std. 1149.1-2001 which are required to support this new I/O test structure.

Other boundary scan test standards (IEEE Std. 1149.1-2001, IEEE Std. 1149.4-1999) do not fully address some of the increasingly common, newer digital network topologies, such as AC-coupled differential interconnections on very high speed (1+ GBps) digital data paths. IEEE Std. 1149.1 structures and methods are intended to test static (that is, DC-coupled), single ended networks. It is unable to test dynamic (that is, AC-coupled) digital networks, since AC-coupling blocks static signals. Differential networks are also inadequately tested by the current IEEE Std. 1149.1-2001, which requires either the insertion of boundary cells between the differential driver or receiver and the chip pads (this often creates an unacceptable performance degradation), or insertion of single boundary cells before the differential driver and after the differential receiver (this reduces controllability and observability to the point that many board assembly defects cannot be detected). IEEE Std. 1149.4-1999 structures and methods are intended for testing analog networks, and in most cases are not able to test these newer digital networks as well. Specifically, IEEE Std. 1149.4-1999 provides the opportunity to inject dynamic (time varying) or analog signals for test, but these structures intended for analog testing are often too intrusive (too high an impact on performance and pin count) for high speed chip designs, and require additional resources and test application time not otherwise required for testing digital circuits. Finally, very high-speed logic imposes new restrictions on test structures that were not considered in IEEE Std. 1149.1. This standard specifies robust and minimally intrusive test structures and methods that provide greater detection and diagnostic capability than existing structures and methods for these classes of digital networks. The standard addresses the physical interface between components, the protocol for sending test data between components and the boundary scan interface. The standard addresses any software and BSDL changes that are required to support this standard.

Applications

- High speed SerDes devices
- All differential I/O (does not need to be AC-coupled - LVDS)
- SPI, Hypertransport and similar interfaces
- Parallel Optics

For more information

On the Web:
http://grouper.ieee.org/groups/1149/6/index.html
Email Group (restricted membership): stds-1149-6wg@ieee.org
Personal Contact: Bill Eklow – Working group chair (beklow@ieee.org)
IEEE 1149.6 web site:

- Simulation results – SPICE simulations of 1149.6 logic with and without fault insertion
- Background information – Provides background on some of decisions made by the working group

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