Measurement of IP Qualification Costs and Benefits

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Abstract

IP core reuse is necessary to overcome the design gap. Yet experience during IP integration has shown that risk is still considerably high when dealing with IPs. IP qualification provides IP providers and integrators with measurable quality characteristics that allow for high quality IP cores and to put buy decisions on a quantifiable basis. This paper presents unprecedented results that facilitate the comparison of the effectiveness of reusing qualified, digital soft IP to previous, immature reuse methods. An impressive reduction in IP integration effort, which is profitable for the IP customer, is demonstrated. Moreover, we show that the IP business can be profitable for the IP provider despite the additional qualification effort.

1. Introduction

During the past few decades, Moore's law has been the justification and driving force for most developments and research in the EDA industry. It is one of the few things which has not changed in this fast-changing environment. Moore's law is still valid with a yearly complexity increase of about 58%. On the other hand, developers' productivity is growing at a far smaller rate of 21%. This positive increase in complexity leads up to the design of a complete electronic system on one single chip. Such systems are also known as System-On-a-Chip (SOC). Because of the productivity gap, it is in the present already a challenge to meet time-to-market within shortening development cycles. In the future it will even be impossible to finish a design successfully unless new design methodologies are adopted [3].

Therefore, in the 90s the reuse paradigm has been introduced to keep pace with Moore's law. It proposes the creation of reusable electronic designs and to use them as basic building blocks for SOC designs. Reusable designs are also called Intellectual Property (IP).

This paradigm helps meeting time-to-market because building an SOC from pre-verified IP is much faster than doing it from scratch. Another advantage is the increased profit due to the reuse of an IP in multiple SOCs, possibly by multiple companies.

Since the late 1990s, a growing market for IP core exchange has been established. IP providers with specific application know-how, for example in audio/video codecs, develop designs that can be reused in an SOC by an IP integrator. IP exchange may take place inside a company (intra-company reuse), but often the IP integrator is a different company whose core competence is system design (inter-company reuse). Engineers had to learn that IP integration is a difficult process with many risks involved. Even if an IP is pre-verified, issues such as design flow incompatibilities could prevent successful IP integration or turn it into a costly process.

This article shows that IP qualification, a set of techniques that help avoid many known issues and maintain high IP quality, makes the IP reuse process much more efficient. Section 2 gives an overview of related work. To elicit the quality level out of an IP core it was first necessary to define an IP quality metric based on industry best practice, which is the subject of section 3. IP qualification methods, which check compliance with IP quality criteria, are introduced in section 4 with emphasis on automated IP qualification for digital soft IP. Section 5 proposes an automatic IP delivery process that enables transfer of qualified IP between design data bases while maintaining qualified properties. Section 6 provides quantitative results that show the benefit measured in person hours from employing a qualification-based IP reuse process. Section 7 concludes the paper.

2. Related work

Technical, business and legal interests must be considered in conjunction with SOC design and reuse of IP cores. The VSIA [7] develops technical methods in order to improve the quality of IP cores and thus eases the integration into a SOC or platform. The VC quality DWG for example develops the Quality IP (QIP) metric. It is in the Reuse Methodology Manual (RMM) [4], too, where rules are defined which lead to the production of quality IP. But all these rules and guidelines have to be checked manually by

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the designer. There is no comprehensive method for IP qualification, which enables an automatic examination of IP cores [9]. For IP licensing and distribution, IP integrators and providers are supported by the work of VSIA and VCX ([7], [10]). However, the IP provider is not supported by tools to show compliance or completeness of its delivery package.

Quality metrics such as OpenMORE [5] support the IP integrator when deciding which of several functionally equivalent IP cores is the one that minimizes risk during integration into a system or platform. However, IP provider and integrator have to assess IP cores manually, which is of course time-consuming and subjective. There are already individual tools available, like rule checkers, code coverage and synthesis tools. Such tools could also be used for the proof of IP quality ([11]-[13]). But it is obvious that an IP qualification flow has to be implemented in order to support several different roles (e.g. IP provider and IP integrator) and to enable quick and efficient IP qualification. Therefore, the following issues are covered by this contribution:

- Proving compliance to design guidelines with the help of automatic tool support.
- Helping the IP integrator to select an IP module by reliable certification.
- Developing an IP qualification methodology which is integrated with an existing design flow.
- Maintaining qualified properties during IP transfer.

3. Quality metrics

A quality metric helps assess the quality of an IP core and thus supports IP buyers in their decision making process. Moreover, it gives IP developers a guideline what quality issues they should focus on. Many IP providers, including sci-worx, have developed internal quality guidelines [15]. Beyond that, standardization of a quality metric is essential for the IP market to expand because it helps IP providers meet customers' needs.

The VSIA's virtual component (VC) quality development working group (DWG), chartered to develop such a standard, has defined IP quality as "the measurable conformance to defined quality characteristics." Following this definition, a quality metric must be composed of the following elements:

- a set of quality characteristics (criteria) C_i,
- a quantification (value set) Q_i for each criterion,
- and a scoring scheme to compute an overall quality value of the IP.

The assessment of an IP block involves the following:

- for each quality criterion, determination and assignment of a quality value $q_i \in Q_i$, and
- Calculation of overall quality q according to the scoring scheme.

An early and prominent approach towards a quality metric has been OpenMORE [5], based on the Reuse Methodology Manual (RMM) [4]. OpenMORE assigns a weight w_i to each criterion C_i: $w_i = 2$ if a C_i is a "guideline", and $w_i = 10$ if C_i is a "rule". Quantification values are 0 (criterion never fulfilled), ½ (sometimes met), 1 (always met). Scoring is performed by computing a weighted sum: $q = \sum_i w_i \cdot q_i$.

This leads to an average quality value; weak quality in some criteria can be compensated by high quality in other areas. Different to that, previous VSIA approaches such as VCT compliance (Appendix D of [6]) and the never published QSS (quality spreadsheet) followed the philosophy that it is always the "weakest link" (quality criterion) that causes a chain (IP) to break, and therefore computed a quality score essentially as the minimum of the individual q_i. Such a metric is very rigid but does not contribute to the differentiation of IPs of similar quality, nor does it allow the IP provider to demonstrate gradual quality improvements.

The authors contributed to the VC quality DWG's new Quality IP (QIP) metric [8], which is in stage of beta test at the time this article is written. For this metric a combined approach has been chosen. The primary metric takes a weighted sum approach with default weights that are adjustable by IP integrators according to their preferences. It is complemented by a weakest link metric that signals whether any of the indispensable or state-of-the-art criteria (called imperatives and rules, respectively) is violated.

Clearly, the overall quality value is best suited for ranking different IPs with respect to quality. Before a buy decision is made, the IP integrator should look into the individual quality criteria to achieve a more detailed understanding of the IP's quality and potential risk.

Key quality criteria, and the qualification of IP with respect to these criteria, are addressed in the following section.

4. Qualification methods

Automatic quality criteria checking is the precondition for an efficient qualification flow. Automated IP qualification speeds up the qualification process, reduces cost, generates objective results and makes results reproducible. Our analysis of VSIA QIP metric reveals that currently ~ 50% of VSIA criteria can be checked automatically (36% full automation, 15% partial automation).

The following subsections describe the qualification steps implemented to check VSIA QIP criteria.

4.1. Completeness of deliverables

The set of deliverables which customers can expect from state-of-the-art soft IP includes, beyond the RTL HDL code, a reference model in C/C++/SystemC, the complete verification environment, scripts and constraints for the major design tools, and documentation as specified in [6]. In sci-worx' IP packages, all the files possess defined names and locations. This makes automated checks of their presence possible. A tool named SDA (sci-worx design structure analyzer) looks up all design and verification files, determines their hierarchical structure, and reports any missing or inconsistent data. Further analysis such as evaluation of the document contents is done manually, guided by checklists.

4.2. Coding guideline and design rule check

RTL coding can influence simulation and synthesis results. Especially for inter-company reuse, where the use of different tools (e.g. for simulation or synthesis) cannot be ruled out, it is important to address RTL coding. sci-worx does this by a set of 313 VHDL coding guidelines and design rules based on RMM and QIP criteria. These guidelines have been refined until they could be implemented with an automated rule checker tool. New generation rule-checkers perform complete RTL code elaboration and fast logic synthesis. Therefore, they are able not only to check compliance to classical RTL coding guidelines, but also to report design rule violations or notify a designer on parts of the design which need special care. This could for instance be a signal that crosses a clock domain boundary.

In this way about 68% of the written rules and guidelines have been implemented. Manual code reviews can now be restricted to the remaining 32% and have become much more efficient.

4.3. Verification qualification

Sufficient simulation, while increasingly improved by formal methods, remains the key verification technique for IP blocks today. The verification environment and test suite can be qualified with respect to the following metrics:

- Code coverage, to understand which sections of the RTL code have been activated by test cases.
- The absolute number and percentage of successfully simulated test cases.
- Development of the bug rate over time.
- Functional coverage, to systematically address typical and corner cases and combinations thereof.

With the exception of functional coverage, these measurements have been implemented at sci-worx. To this end, it was necessary to standardize the structure of verification environments and the set-up of test cases for all IPs. Moreover, a bug tracking system had to be installed.

4.4. Synthesis qualification

High-quality synthesis results cannot sufficiently be ensured by RTL code checking. Even for soft IP, which is delivered as RTL source code to an IP integrator, a full synthesis to a sample technology is carried out. Custom post-processing tools automatically ensure the absence of synthesis errors and analyze synthesis reports with respect to, e.g., gate count and maximum operation frequency. Through the automated invocation of scan path synthesis and test pattern generation (ATPG), "stuck at" fault coverage is determined. If specified coverage, gate count and frequency results are not achieved, a design iteration is initiated (cf. "short loop" in section 6).

Synthesizability is an important quality criterion but it needs to be accompanied by a functional correctness check. A formal gate level netlist vs. RTL code verification ensures the post-synthesis functional accuracy of the IP core as part of the qualification process.

4.5. Qualification framework

All qualification tools are embedded into the common framework depicted in Figure 1. The framework extracts the design structure from the set of design files and provides mechanisms to invoke the selected qualification steps. From the resulting log files, summaries are created and can be referenced in the qualification report. If issues not documented by the designers are detected, a design iteration is considered.

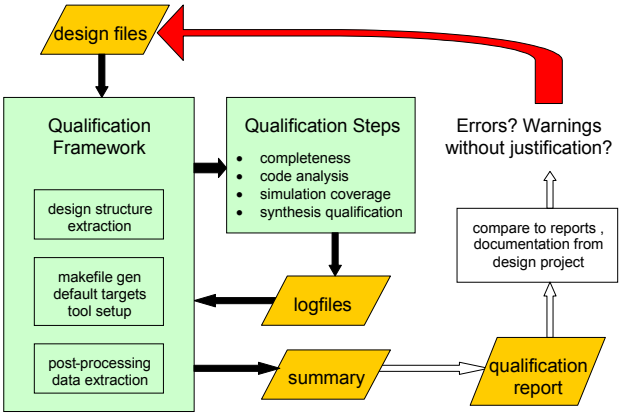

Figure 1: Automated qualification framework

Initially, the qualification framework had been used primarily by sci-worx' IP department when qualifying sci-worx own IP or importing third party IP. By making it available to all designers, they are now in the position to pre-qualify their work before final certification. Thanks to automation, overhead is limited while on the other hand design iterations and the incurred cost are reduced.

5. IP delivery automation

IP delivery automation enables automatic mapping between different IP core structures. In the majority of cases for inter-company reuse IP content databases of IP provider and IP integrator will differ in format. These internal formats cannot easily be changed because in most cases the reuse database format reflects the file/directory structure used during IP development and IP integration. To this company-internal structure, the design flow and therefore tool configurations are adapted. The sensitive tool tuning is something that neither IP provider nor IP integrator are willing to interfere with.

Current IP core designs contain hundreds of files with dependencies; e.g. synthesis scripts depend on HDL files, test bench files build on I/O pattern files, etc. Analysis of VSIA QIP revealed that 27% of the (semi-)automatically checkable rules are related to file and directory structure. To achieve high quality IP it is crucial to account for these dependencies when transferring IP.

Because of different file/directory structures and file dependencies, importing an IP core into the reuse database needs about one person-week for a medium size IP core. It takes so long due to the fact that the import process is done manually. The amount of time has to be multiplied by the number of third party IP cores that will be integrated into the SOC and the number of updates. Hence, automation of the IP delivery process will be profitable.

IP core handoff between IP provider and integrator has to be based on a common format on which both parties are able to agree on IP quality. It also has to be guaranteed that IP integrity of a qualified IP core is fulfilled after IP packaging and IP import.

A general format as basis for automated quality checks and IP transfer promises to be the solution for the above mentioned gaps. Figure 2 shows how IP core handoff can be applied during the transfer process on the basis of a general format. Also other tool flows will benefit from a general IP content format. The requirement for such a format is that neither IP provider nor IP integrator have to change their internal formats because of the reasons given above. Therefore, it is necessary to have a general intermediate format which is known by both parties. A key requirement for automatic mapping between the two formats, transfer and IP integrator's (IP provider's) content database format is that they are well defined. This means a company-wide uniform IP core file/directory structure is prerequisite. This requirement is fulfilled by most IP providers, even if only minor quality requirements are taken into consideration. Additionally higher-level meta data have to be added to the pure file/directory structure for mapping purposes.

HDL files, simulation (scripts, input and output patterns, etc.), synthesis environment (scripts, reports, constraints, etc.) and documentation, etc. are called the IP content. IP content is that which will be integrated into an SOC design and it is embedded in a bigger context: the IP qualification (IPQ) format. The IPQ format fulfills the above-mentioned requirements and includes all data that will be transferred from an IP provider to an IP integrator (Figure 2).

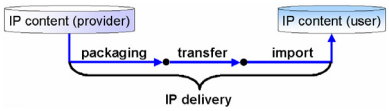

Figure 2: IP delivery process

The IPQ format is described in XML schema [14]. The IP content part of the XML description includes the above mentioned mapping meta data as well as information about the tools used during IP core development (see XML code example below). This information supports a straightforward IP instantiation at the IP integrator's site.

```
<PhysicalUnit name="vhdl" xsi:type="Directory">
  <PhysicalUnit name="file.vhd" xsi:type="File">
    <LogicalUnit version="0.1" toolname="XEmacs"
      toolversion="21.4.13" isExecutable="false"
      xsi:type="VHDL">
      <LogicalRole name="RTL" xsi:type="RTL"/>
      <LogicalPart name="entity_name"
        xsi:type="entity"/>
    </LogicalUnit>
```

Due to this information the import tool will guide the IP integrator by identifying the right setup scripts for these tools. A setup script prepares the environment so that the tool can be used. Among the typical tasks performed by a setup script are: environment variables are set, the path variable is set or modified, etc. These actions are only site and tool dependent. This means that a setup script does not include IP core specific information. Therefore, it is recommended not to transfer setup scripts, but to provide instantiation support, which allows accessing the site and tool dependent setup scripts.

Necessary mapping information for IP packaging and IP import (Figure 2) is provided either by the companies themselves or via a central database (Figure 3). In the later case, modifications to the local tools at the IP provider's and integrator's side are reduced to a minimum. The database can be maintained by an IPQ format consortium that also has to maintain the IPQ format itself and to decide whether modifications to the format are necessary to adapt it to future needs.

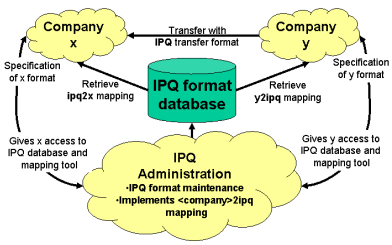

Figure 3: IPQ format database

The IPQ content format does not require a tool API. Due to file/directory structure mapping, tools can access files directly. The disadvantage is that during structure mapping IP core accompanying scripts (e.g. scripts for synthesis, simulation, etc.) become invalid.

This is due to the already mentioned dependencies between IP core files, which will be sorted into a different structure. Therefore, file and path names in scripts and configuration files have to be adapted to the modified structure. These adaptations will ensure an executable IP core. After analysis of some IP cores a good coverage can be reached if C-shell, Perl, Tcl, synthesis scripts, VHDL test benches, VERILOG test benches, and C, C++ files are addressed.

The adaptation challenge will be further pursued.

6. Results

The improvement made possible by applying the techniques presented in this paper has been measured in a series of projects at sci-worx that involve a peripheral interface block. All data has been extracted from the project effort database where engineers book their effected hours of work.

Before the ToolIP project [2], a common approach to IP reuse was to extract a block that had been developed earlier in an application project, and to import and integrate that block into a reuse project (cf. Figure 4). The drawback consisted in the fact, as column 1 of Table 1 shows, that the effort for extraction and integration could well exceed the initial development effort of that block. It would have been cheaper to develop that block from scratch again. Even in the case of multiple reuse, this approach would have been uneconomical due to repeated extraction and re-engineering activities.

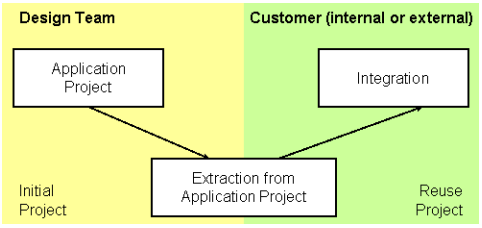

Figure 4: Immature Reuse Process

Since 2002, a reuse process developed in the ToolIP project (Table 1) has increasingly been employed at sci-worx. After the positive evaluation of a block's market potential, a block is improved so that it meets defined IP quality criteria (cf. Section 2). Using the techniques from Section 4, the block is qualified by a separate organizational unit, IP Publishing. This may lead to design iteration ("short loop") if further enhancements are needed. If the block is suitable, it is called DesignObject and checked in into an IP repository from which it is delivered to customers. IP publishing provides first level support to deal with customer feedback and claims. If this is not sufficient, a design iteration must be initiated. Since this iteration involves the customer, it is termed "long loop".

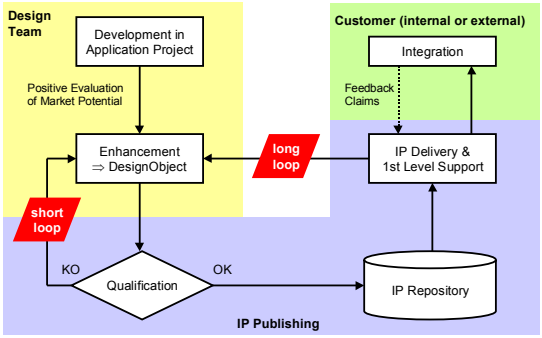

Figure 5: sci-worx Reuse Process

The effort data for the initial development, for making the design reusable according to the quality criteria, and for the actual reuse are listed in column 2 of Table 1. Obviously, the effort for preparing a reusable core is significant, and total person-power for one reuse is even slightly higher than with the immature reuse process. However, the integration effort is reduced by 95%. Hence, the IP integrator (customer) has a large benefit from the application of IP qualification methods by the IP provider.

Table 1: Effort data for several reuse scenarios of a peripheral interface block

Column No.	1	2	3	4
Scenario	immat. 1st reuse [Ph]	ToolIP 1st reuse [Ph]	ToolIP 2nd reuse [Ph]	ToolIP fully deployed [Ph]
Initial Dvlpmt	2340	2340		2500
Enhancement		2300		1000
Qualification		45	10	10
Delivery&Supp.		350	16	16
Integration	2450	120	100	100
Total	4790	5155	126	3626

We now discuss whether IP reuse based on the process devised in Table 1 is economical when taking the provider's effort (cost) into account. This requires more than a single reuse. At sci-worx, the peripheral IP core has been reused a second time. This involved a re-qualification to account for the improvements made in the support phase of the first reuse, delivery to the target project, and IP integration. Effort (see column 3 of Table 1) was small since no extraction, improvement, and re-engineering was necessary. Had we attempted a second reuse with the previous, immature approach, we would have effected again about 2000 person-hours.

The reuse process allows an IP provider to operate as follows in order to reduce risk to a minimum:

- Develop a block on demand in an application project, e.g. with a lead customer. At this point, there is no investment into making the block ready for reuse.
- When an IP customer is in sight, prepare a high quality IP by enhancing and qualifying the block. At this point, the provider is unlikely to make a profit since the revenue is consumed by the additional development cost. However, company value is increased thanks to the IP in the shelf.
- Upon second and further reuse of the IP, business becomes profitable.

Note that in this research, the initial development was without IP quality in mind. As ToolIP results are promoted in the company, engineers persuaded to design reuse-ready right from the start, and automated qualification tools based on the method presented in section 4 available to every designer, we expect slightly higher effort for initial development, but significant reduction of the further steps towards a DesignObject. An estimate is given in column 4 of Table 1.

Statistics about claims made to sci-worx' customer support show that IP qualification has helped to reduce the number of "long loops" significantly (Figure 6). The customer benefits from reduced time-to-market risk, and sci-worx from less effort for the rectification of rejects.

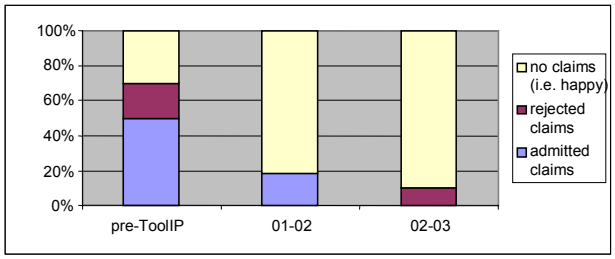

Figure 6: Percentage of IP deliveries involving claims

7. Conclusions

This paper presents an automatic qualification framework in which several qualification methods, like completeness check, coding guidelines and design rule checks, verification and synthesis qualification are implemented. This makes it possible to automatically check ~50% of the IP core's quality criteria defined by the VSIA QIP metric.

The value of the quality framework is shown by an up to 95% integration effort reduction, the prospect of further benefits due to the use of qualification methods right from the start and less customer claims.

Finally, it is important to remark that this research is based on an intra-company IP exchange. The techniques presented in Section 5 are essential in order to avoid additional effort on the customer side due to the need to adapt the IP structure to the customer's conventions regarding design data organization. Therefore, a transfer of the results also to inter-company reuse projects should be feasible.

8. Acknowledgments

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References

[1] IPQ, BMBF IPQ project website, Website (Dez. 2000). URL http://www.ip-qualifikation.de

[2] ToolIP, MEDEA+ ToolIP (A511) project website, Website (Jan. 2001). URL http://toolip.fzi.de

[3] Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors (ITRS), Website (2001). URL http://public.itrs.net/Files/2001ITRS/Home.htm

[4] P. Bricaud, M. Keating, Reuse Methodology Manual for System-on-a-Chip Designs Second Edition, Kluwer Academic Publishers, 1999.

[5] Synopsys, Inc. and Mentor Graphics, OpenMORE, Website (1998). URL http://www.openmore.com

[6] Virtual Socket Interface Alliance (VSIA), VSIA Deliverables Document (May 2002). URL http://www.vsi.org/resources/TechnicalDocumentsList.htm

[7] Virtual Socket Interface Alliance (VSIA); VSIA Homepage; 2003; http://www.vsi.org.

[8] Virtual Socket Interface Alliance (VSIA), QIP Quality Metric. To be published, end 2003.

[9] Seepold, R.; Martínez Madrid, N.; (eds.); Virtual Components Design and Reuse; Kluwer Academic Publishers; December 2000; ISBN 0-7923-7261-1.

[10] Virtual Component Exchange (VCX); VCX Homepage; 2003; http://www.vcx.org.

[11] Y. Torroja, F. Casado, F. Machado, T. Riesgo, E. de la Torre, and J. Uceda, "Using a Simplified Hardware Model to Analyse the Quality of VHDL Based Designs" in User Forum at DATE, Paris (France), February 2000.

[12] J. Schneider, S. Rülke, and A. Reutter, "Comparison of Different Analysis Approaches for Coding Guidelines and Implementation of a TCL-based Prototype" in Proceedings of FORUM on DESIGN LANGUAGES (FDL'2000), September 4-8, 2000, University of Tuebingen, Germany

[13] Tsu-Hua Wang, Chong Guan Tan, "Practical code coverage for Verilog", in Proceedings of 4th IEEE International Verilog HDL Conference, March 27 - 29, 1995, Santa Clara, CA, Page 99

[14] M. Schaaf, M. Visarius, R. Bergmann, R. Maximini, M. Spinelli, J. Lessmann, W. Hardt, S. Ihmor, W. Thronicke, C. Tautz, R. Traphoener, "IPCHL - A Description Language for Semantic IP Characterization" at Forum on Design Languages 2002, Marseille, September 2002

[15] R. Goering, P. Clarke "Design reuse on a macro level", 1998 http://www.eetimes.com/news/98/1020news/rmm2.html