A Compact Propagation Delay Model for Deep-Submicron CMOS Gates including Crosstalk

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Abstract- **We present a compact, fully physical, analytical model for the propagation delay and the output transition time of deep-submicron CMOS gates. The model accounts for crosstalk effects, short-circuit currents, the input-output coupling capacitance and carrier velocity saturation effects. It is based on the nth-power law MOSFET model and computes the propagation delay from the charge delivered to the gate. Comparison with HSPICE simulations and other previously published models for different submicron technologies show significant improvements in terms of accuracy.**

I. Introduction

Timing analysis is one of the most important topics in VLSI design. The nonlinear behavior of CMOS gates requires numerical procedures for accurate timing analysis that together with today's circuit complexity results in large computation times. Moreover, the constant scaling of feature sizes and supply voltages with the increase in both operating frequency and signal rise/fall times has made digital designs more vulnerable to noise. In modern ICs, interconnect coupling noise (crosstalk) becomes a performance limiting factor that must be analyzed carefully during the design process. If not considered, crosstalk can cause extra delay, logic hazards and logic malfunction.

Traditionally gate delay and crosstalk have been treated as independent problems and modeled separately. The impact of crosstalk on gate delay for scaled technologies requires a compact gate delay model that incorporates this effect for an optimized analysis.

The propagation delay of CMOS inverters has been extensively studied in the past [1]-[7] as a first step to describe more complex gates [8, 9]. Cocchini et al. [3] obtained a piece-wise expression for the propagation delay based on the BSIM MOSFET model [10]. The model included overshooting effects (due to the input-to-output coupling capacitance) while short-circuit currents were neglected. In [2] and [4] K.O Jeppson and L. Bisdounis presented a model for the output response of CMOS inverters using a quadratic current-voltage dependence for MOSFET devices, which is not longer valid for submicron and deep-submicron devices. Daga et. al. [5] obtained a simple empirical expression for the propagation delay taking into account both overshooting and short-circuit currents. Although the simplicity of their model, there is a lack of physical meaning due to the use of fitting parameters. Hirata et al. [6] derived a delay model based on the α-power law MOSFET model developed by Sakurai and Newton [11] considering both short-circuit and overshooting currents. The model provides an accurate description for the propagation delay but the computation time is severely increased due to the adoption of numerical procedures in the analysis. Bisdounis et al. [7] developed a piece-wise solution with seven operation regions for the transient response of a CMOS inverter. The model is also based on the α-power law MOSFET model [12] and includes both overshooting and short-circuit currents. T. Sakurai et. al. [8] obtained a simple expression for the propagation delay of CMOS gates based on their *nth*-power law MOSFET model neglecting both short-circuit and overshooting currents.

Crosstalk delay was analyzed in [13] using a waveform iteration strategy, and therefore no-closed form expression for the worst-case victim delay could be provided. More recently crosstalk delay has been modeled analytically in [14] to quantify the severity of crosstalk delay and describe qualitatively its dependence on circuit parameters like the rise/fall times of transitions. The nMOS (pMOS) network is substituted by a pull-down (pull-up) resistance and the short-circuit currents are neglected. The main limitation of this approach is that the complex equations obtained for the victim voltage variation cannot be used to obtain a closed-form expression of the propagation delay. Additionally, other effects as short-circuit currents, that have a significant impact on the propagation delay are not considered.

In this work we present a gate delay model that includes crosstalk and accounts for the main effects in deep-submicron technologies as the influence of the input-output coupling capacitance, the carriers velocity saturation and short-circuit currents. The use of fitting parameters is avoided to provide a complete physical description. The delay is computed from the charge that is transferred from the supply node to the output of the gate (for a low-high output transition) or from the output to ground (the high-low output transition case). This approach facilitates the description of complex effects like crosstalk without any kind of penalty in terms of computation time. Comparisons with respect to HSPICE simulations and other previously published models for different technologies show significant improvements.

This paper is organized as follows: In Section 2 the CMOS inverter switching characteristics are analyzed

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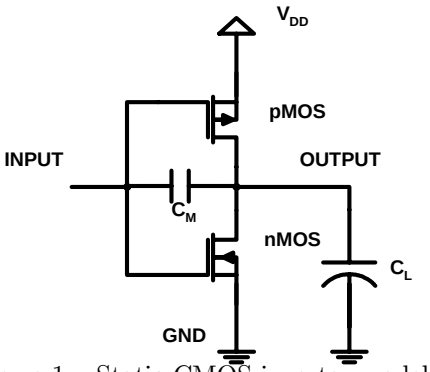

Figure 1 – Static CMOS inverter model.

and the MOSFET model used is presented. The delay and the output transition time models are developed in Section 3 and compared to HSPICE simulations and other previously published models for different technologies in section 4. Finally in section 5 we present the conclusions.

II. Analysis of the CMOS inverter switching characteristics

The dynamic behavior of a CMOS inverter (see Fig.1) is described by:

$$(C_L + C_M)\frac{dV_{out}}{dt} = I_p - I_n + C_M\frac{dV_{in}}{dt} \qquad (1)$$

where C_L is the output capacitance, V_{out} and V_{in} are the output and input voltage respectively, while I_p and I_n is the current that crosses the pMOS and the nMOS transistor respectively. C_M is the input to output coupling capacitance which is voltage dependent. The static value of C_M when the input is low (C_M^L) is computed considering the side-wall capacitances of both transistor drains and the gate to drain capacitance of the pMOS transistor that operates in the linear region as:

$$C_M^L = C_{ox}\left(\frac{W_{p_{eff}}L_{p_{eff}}}{2} + L_{D_p}W_{p_{eff}} + L_{D_n}W_{n_{eff}}\right) \qquad (2)$$

with $W_{p_{eff}}$ and $W_{n_{eff}}$ being the effective channel width of pMOS and nMOS respectively, $L_{p_{eff}}$ is the effective channel length of pMOS, while L_{D_n} and L_{D_p} are the gate-drain underdiffusion for the nMOS and pMOS transistors respectively. For a static input high the capacitance C_M^H is obtained similarly. In this work a mean value for the coupling capacitance during the transition ($C_M = 0.5\left(C_M^L + C_M^H\right)$) is used.

The propagation delay (defined as $t_{p_{HL}}$ for a high to low output transition) is typically defined as the time interval from the 50% V_{DD} input voltage to the 50% V_{DD} output voltage. The dependence of the propagation delay with design parameters is non-linear and difficult to model given that (1) can not be solved in a closed form even using the simple Shockley MOSFET model. Moreover carrier saturation effects become important with technology scaling and more complex MOSFET models accounting for such effects must be considered. The influence of a switching coupled line (crosstalk), would require an additional differential equation coupled to (1), thus complicating the analysis more severely.

The *nth*-power law MOSFET model [11] is a widely used short-channel drain current model, and will be used in this work to derive the propagation delay and the output transition time of CMOS inverters. The drain current is expressed as:

$$I_D = \begin{cases} 0 & (V_{GS} \leqq V_{TH}) \\ (2 - \frac{V_{DS}}{V'_{D0}})\frac{V_{DS}}{V'_{D0}}I'_{D0} & (V_{DS} < V'_{D0}) \\ I'_{D0} & (V_{DS} \geqq V'_{D0}) \end{cases} \qquad (3)$$

with

$$I'_{D0} = I_{D0}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^n \qquad (4)$$

where V_{GS} ,V_{DD}, and V'_{D0} are the gate, supply, and saturation voltage respectively and I_{D0} is the drain current at $V_{GS} = V_{DS} = V_{DD}$. The parameter n is the velocity saturation index that ranges between 2 (long-channel devices) and 1 (short-channel) [11]. The saturation voltage V'_{D0} is given by:

$$V'_{D0} = V_{D0}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^m \qquad (5)$$

The parameter V_{D0} is the saturation voltage at $V_{GS} = V_{DD}$, while m and V_{TH} are empirical parameters in [11]. These equations are mathematically simpler than physically-based MOSFET models such as BSIM3v3 or MM9 with the disadvantage that, in the original model developed by Sakurai and Newton, the relationship between the empirical and the process parameters supplied by manufacturers is not provided. The variation of the *nth*-power law model predictions with key parameters like the supply voltage or temperature is not taken into account in the original formulation performed by Sakurai and Newton, where each parameter must be recomputed if the supply voltage, the temperature of operation, or some device dimension are changed. In this work we use the physical formulation for the *nth*-power law developed previously [15]. Using this formulation, the empirical parameters used by Sakurai et. al can be related to physical parameters like the supply voltage or temperature.

III. Propagation Delay Model for CMOS Inverters

We compute the propagation delay when the input voltage rises (for a falling transition the analysis is equivalent). The short-circuit, overshooting, and crosstalk effects are first neglected and incorporated later. Assuming a linear variation of the input voltage with rise time t_{in} and using the *nth*-power law model the analytical solution for the output voltage valid while the nMOS is saturated ($V_{out} > V'_{D0_n}$) is:

$$V_{out} = V_{DD} - \frac{I_{D0_n}}{C_L}\left(\frac{t - t_n}{t_{in} - t_n}\right)^{n_n+1}\frac{t_{in} - t_n}{n_n + 1} \qquad (6)$$

where parameters I_{D0_n} and n_n are the maximum saturation current and the velocity saturation index of nMOS respectively. Parameter t_n is the time at which the

nMOS starts to conduct. From (6) we obtain the time at which the output voltage is $V_{DD}/2$. Then the propagation delay will be this time minus the time at which the input is also at $V_{DD}/2$ (i.e. $t_{in}/2$):

$$t_{pHL_1} = t_n + \left[\frac{Q_f\,(n_n+1)}{I_{D0_n}}\right]^{\frac{1}{1+n_n}} (t_{in}-t_n)^{\frac{n_n}{n_n+1}} - \frac{t_{in}}{2} \tag{7}$$

where $Q_f = C_L V_{DD}/2$ is the charge transferred by the nMOS transistor when the output reaches $V_{DD}/2$. Equation (7) is valid for slow inputs (defined when $t_{pHL} \leq t_{in}/2$) since for fast inputs the nMOS transistor is not saturated when the output reaches $V_{DD}/2$. If Q_{f_0} is defined as the total charge transferred through the nMOS transistor when $t_{pHL} = t_{in}/2$ (the limit between fast and slow input transitions), then (7) is valid when $Q_f \leq Q_{f_0}$. The value of Q_{f_0} is obtained equating $t_{pHL_1} = t_{in}/2$ and solving for Q_{f_0}

$$Q_{f_0} = \frac{I_{D0_n}}{(n_n+1)} t_{in}\left(1 - \frac{V_{TN}}{V_{DD}}\right) \tag{8}$$

where V_{TN} is the threshold voltage of nMOS. For fast input transitions, the input reaches the supply voltage before the output is at $V_{DD}/2$ and then $Q_f > Q_{f_0}$. For this case (7) is not valid and the propagation delay is obtained by solving (1) for $I_n = I_{D0_n}$ (also neglecting the short-circuit and the overshooting currents as a first analysis) leading to:

$$t_{pHL_2} = \frac{t_{in}}{2} + \frac{Q_f - Q_{f_0}}{I_{D0_n}} \tag{9}$$

Equation (9) is valid for the interval $Q_f > Q_{f_0}$ (fast input range). For simplicity, the proposed model for the propagation delay (eqs. (7) and (9)) does not take into account the fact that the nMOS transistor enters in its linear region in the interval $V_{DD}/2 < V_{out} < V'_{D0_n}$ for those cases in which $V'_{D0_n} > V_{DD}/2$.

The output fall time (t_f), defined as the 70% of the output voltage slope at $V_{DD}/2$ [8], is obtained in a similar way as (7) and (9). The output voltage slope takes the form:

$$\left.\frac{dV_{out}}{dt}\right|_{V_{DD}/2} = \begin{cases} -\frac{I_{D0_n} V_{DD}}{2Q_f}\left(\frac{Q_f(n_n+1)}{(t_{in}-t_n) I_{D0_n}}\right)^{\frac{n_n}{n_n+1}} & (Q_f < Q_{f_0}) \\ -\frac{I_{D0_n} V_{DD}}{2Q_f} & (Q_f > Q_{f_0}) \end{cases} \tag{10}$$

For the evaluation of the output fall time we use:

$$t_f = \frac{V_{DD}}{\left.\frac{dV_{out}}{dt}\right|_{V_{DD}/2}} \tag{11}$$

The value of the output fall/rise time is needed for the evaluation of the input fall/rise time of the gates driven by the inverter.

A. *Including short-circuit currents*

The model developed cannot be used for static CMOS gates since the short-circuit current was not considered

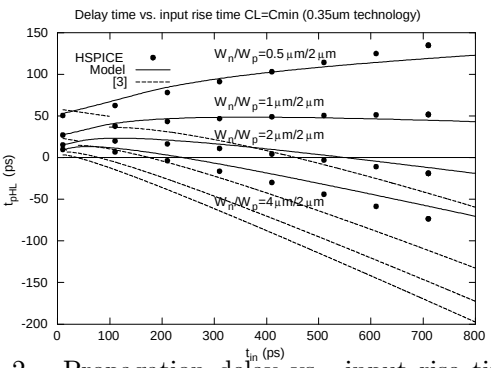

Figure 2 – Propagation delay vs. input rise time for different values of the configuration ratio. Short-circuit currents are not taken into account in [3]

(I_p was neglected when solving (1)). In general, the impact of the short-circuit current on the gate delay can be considerable, specially for large values of the input time. In Fig.2 we plot the propagation delay $t_{p_{HL}}$ vs. the input time t_{in} for different values of the W_n/W_p ratio for a $0.35\mu m$ technology. HSPICE simulations (dots) are compared to a previous model [3]. Short-circuit currents were not taken into account in [3], leading to severe underestimations of the propagation delay for large values of t_{in}. The difference between simulations and the model developed in [3] can be associated to the delay increment due to short-circuit currents.

In this work, the short-circuit current contribution to the gate delay is modeled as an additional charge transferred through the pull-down (pull-up) transistor during an output falling (rising) transition. We develop an analytical expression for the short-circuit charge transferred when the output capacitance is negligible (the case where the impact of short-circuit current on the propagation delay is higher). In this case, the circuit behavior is close to the inverter DC operation since $I_p \simeq I_n$. At the beginning of the transition, the pMOS transistor drives a current equal to the nMOS saturation current, while at the end of the transition the pMOS is saturated. The time point at which the maximum current takes place is such that $I'_{D0_p} = I'_{D0_n}$. We compute the short-circuit charge transferred until this switching point. Given that $V_{GS} = V_{in}$ for the nMOS and $V_{GS} = V_{DD} - V_{in}$ for the pMOS, the time at which the short-circuit is maximum (defined as $t^{CL=0}_{\max}$) is obtained solving:

$$I_{D0_n}\left(\frac{V_{DD}\frac{t^{CL=0}_{\max}}{t_{in}} - V_{TN}}{V_{DD}-V_{TN}}\right)^{n_n} = I_{D0_p}\left(\frac{V_{DD}-V_{DD}\frac{t^{CL=0}_{\max}}{t_{in}} - |V_{TP}|}{V_{DD}-|V_{TP}|}\right)^{n_p} \tag{12}$$

where I_{D0_n} and I_{D0_p} are the parameters I_{D0} of the nMOS and the pMOS transistor respectively, and V_{TP} is the threshold voltage of the pMOS. We obtained a good analytical approximation to the solution of (12) as:

$$t_{\max}^{C_L=0} = t_n + t_{in}\frac{\left(1-\frac{V_{TN}}{V_{DD}}-\frac{|V_{TP}|}{V_{DD}}\right)}{1+F_p^{\frac{2}{n_p+n_n}}} \quad (13)$$

where F_p is given by:

$$F_p = \frac{I_{D0_n}}{I_{D0_p}}\left(\frac{V_{SC}}{V_{DD}-V_{TN}}\right)^{n_n}\left(\frac{V_{DD}-|V_{TP}|}{V_{SC}}\right)^{n_p} \quad (14)$$

where $V_{SC} = V_{DD} - V_{TN} - |V_{TP}|$. The short-circuit charge transferred until $V_{out} = V_{DD}/2$ is computed integrating the nMOS current from the time point at which the nMOS starts to conduct (t_n) until the time point at which the short-circuit is maximum ($t_{\max}^{CL=0}$). From this integration we have:

$$q_{sc}^f = \frac{I_{D0_n}t_{in}}{1+n_n}\left(\frac{1-\frac{V_{TN}}{V_{DD}}-\frac{|V_{TP}|}{V_{DD}}}{1+F_p^{\frac{2}{n_p+n_n}}}\right)^{n_n+1}\left(\frac{V_{DD}}{V_{DD}-V_{TN}}\right)^{n_n} \quad (15)$$

Finally, the value of the charge transferred through the nMOS during the falling output transition used in the delay model is $Q_f = C_L V_{DD}/2 + q_{sc}^f$.

Note that $q_{sc}^f < Q_{f_0}$. For large values of the output capacitance (C_L) such that the transitions is in the fast input range ($Q_f > Q_{f_0}$), eq. (15) is not valid. The additional charge in the fast input range due to (15) in Q_f is negligible with respect $C_L V_{DD}/2$. For this reason we decide to use (15) for all cases since when (15) is not valid the impact on the delay due to the inclusion of q_{sc}^f in Q_f is negligible and the total delay is practically not affected.

B. Modeling CMOS Gates

Complex CMOS gates are modeled through a gate collapsing technique. Each stack of transistors is collapsed into a single equivalent transistor. The maximum current of this single equivalent transistor would be the maximum current of the stack. For the case of a stack of nMOS transistors we define $I_{D0n}^{\langle 1,N_n\rangle}$ as the maximum current that can be driven by the stack (modeled as a chain of N_n series-connected transistors) that is obtained from the transistor collapsing technique developed in [9]. For the simple case of a chain with N_n identical transistors, the collapsing technique provides a simple expression for $I_{D0n}^{\langle 1,N_n\rangle}$:

$$I_{D0n}^{\langle 1,N_n\rangle} = \frac{I_{D0n}}{1+(N_n-1)K_n} \quad (16)$$

where I_{D0n} is the maximum saturation current of each nMOS (drain current when $V_{GS} = V_{DS} = V_{DD}$). The parameter K_n is a technology-dependent parameter given by:

$$K_n = \frac{3V_{D0_n}n_n(1+\gamma_n)}{5(V_{DD}-V_{TN})} \quad (17)$$

where γ_n is the body effect parameter of nMOS.

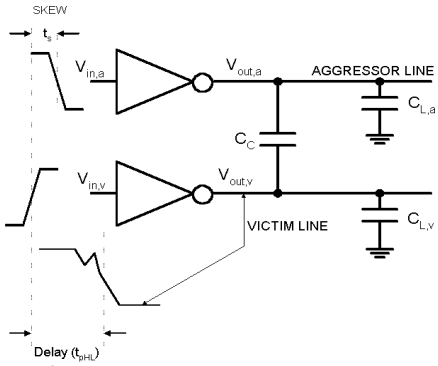

Figure 3 – An additional delay in the victim is induced by the switching transition of $V_{out,a}$ (crosstalk induced delay).

C. Including overshooting and crosstalk

Similarly to short-circuit current, the impact of the overshooting current on the delay is included as an additional charge to be transferred through the nMOS transistor. For fast inputs, the charge injected through the coupling capacitance (C_M) when $V_{out} = V_{DD}/2$ is $Q_{ov} = C_M V_{DD}$. For simplicity we assume the same value for Q_{ov} in the slow-input case. Therefore, the total charge to be transferred through the nMOS transistor during a falling output transition is computed as:

$$Q_f = 0.5\left[\left(C_L + 2C_M\right)V_{DD}\right] + q_{sc}^f \quad (18)$$

The crosstalk induced delay is also considered as an additional charge to be transferred through the charging (discharging) transistor. Crosstalk affects delay when two lines (the aggressor and the victim) switch simultaneously. For a victim node falling transition, the gate delay can be reduced (this lower bound is defined as $t_{pHL,su}$) or increased (defined as $t_{pHL,sd}$) depending on if the aggressor makes a falling or a rising transition respectively. Since large circuits can handle hundreds of millions of interconnect lines on a single chip, simple and accurate analytical descriptions for crosstalk delay are of high importance for a fast timing verification of the whole chip. Consider the circuit in Fig.3 where the aggressor and the victim gates drive an output capacitance $C_{L,a}$ and $C_{L,v}$ respectively, and there is a coupling capacitance C_c between $V_{out,a}$ and $V_{out,v}$ (that causes the crosstalk between the two lines). The total capacitance at the output of the victim gate that must be charged and discharged is the addition of $C_{L,v}$ and C_c. We estimate the crosstalk delay bounds considering that the whole aggressor switching happens within the switch interval of the victim line. For the case of opposite (identical) transitions in both nets, a charge $C_c V_{DD}$ ($-C_c V_{DD}$) is injected through the coupling capacitance from the aggressor to the victim line. We add these additional charges to the charge-based delay model developed to obtain the crosstalk delay bounds.

$$Q_f^{\pm} = 0.5\left[\left(C_{L,v} + C_c + 2C_M\right)V_{DD}\right] + q_{sc}^f \pm C_c V_{DD} \quad (19)$$

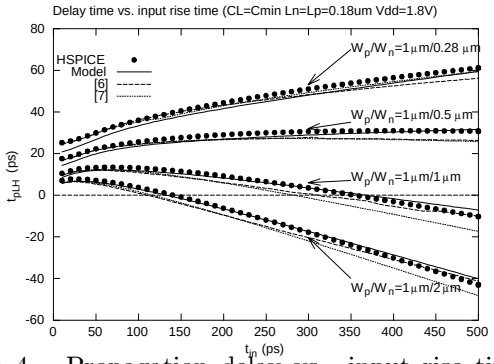

Figure 4 – Propagation delay vs. input rise time for different values of the configuration ratio.

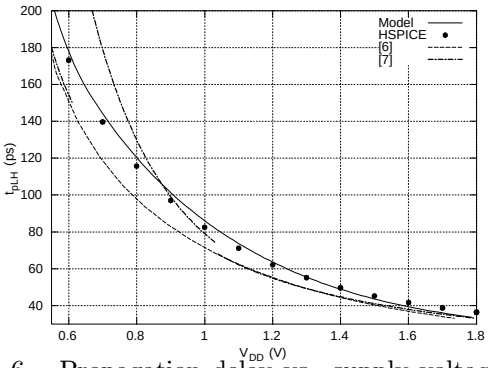

Figure 6 – Propagation delay vs. supply voltage for a $0.18\mu m$ technology.

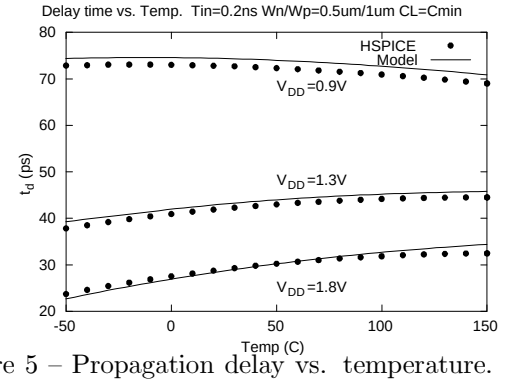

Figure 5 – Propagation delay vs. temperature. Different delay trends vs. temperature can be appreciated at different supply voltages.

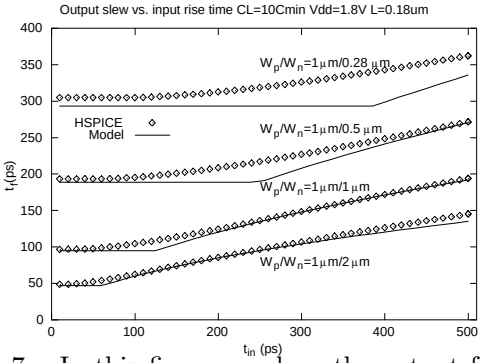

Figure 7 – In this figure we show the output fall time dependence with the input rise time for a $0.18\mu m$ technology.

Equation (19) must be used in eqs. (7), (9) and (11) to estimate the propagation delay and the transition time of the gate.

IV. Results

We plotted model results vs. HSPICE simulations for different technologies, and provide the propagation delay for different values of the input transition time t_{in}, the configuration ratio W_p/W_n, and the supply voltage V_{DD}.

In Fig.2 we plot the crosstalk-free propagation delay $t_{p_{HL}}$ vs. the input time t_{in} for different values of the W_n/W_p ratio for a $0.35\mu m$ technology. HSPICE simulations (dots) are compared to the model proposed obtaining a good accuracy.

Fig.4 plots the crosstalk-free propagation delay vs. the input rise time for a $0.18\mu m$ technology. When the W_p/W_n ratio is small the propagation delay decreases when increasing the input rise time. The model proposed in this work (solid lines) and the previously-published in [6, 7] provide a good approximation to HSPICE simulations (dots).

In Fig.5 we show the propagation delay variation with temperature for three different supply voltage values. Different trends are observed for each supply voltage value when increasing temperature. The propagation delay increases for $V_{DD} = 1.8V$ while for $V_{DD} = 0.9V$ the propagation delay decreases. This effect is described properly by the proposed model since we are using the physically-based nth-power law MOSFET model developed in [15] that relates the nth-power law parameters to physical parameters (that are temperature-dependent) as the carrier mobility. For a more detailed description of this model the reader is referred to [15].

Fig.6 is a plot of HSPICE simulations (dots) and model predictions of the propagation delay vs. the supply voltage (crosstalk is not considered). The model proposed in this work provides a better fitting than the models in [6, 7]. The model in [7] present discontinuities due to the use of different expressions for the propagation delay.

In Fig.7 we plot HSPICE simulation of the output transition time t_f for different values of the input rise time t_{in} and the configuration ratio W_p/W_n. A maximum relative error of 15% is obtained between model predictions and HSPICE simulations. In general a good agreement is obtained with the proposed model.

In Fig.8 we plot the propagation delay limit bounds for a 3-NAND gate for different values of the coupling to load capacitance ratio $C_c/C_{L,v}$. Fig.8 shows an excellent agreement between HSPICE simulations (dots) and the proposed crosstalk delay model (lines).

V. Conclusions

We have developed an accurate analytical expression to compute the propagation delay and the output tran-

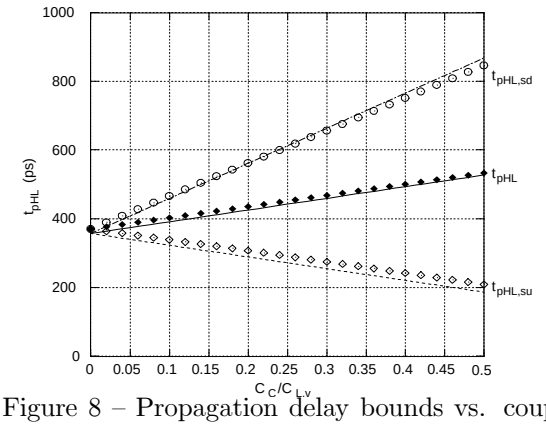

Figure 8 – Propagation delay bounds vs. coupling capacitance. Solid lines are model predictions while dots are HSPICE simulations.

sition time of CMOS gates including crosstalk effects. The main effects present in current submicron CMOS technologies like the input-output coupling capacitance, carriers velocity saturation effects and short-circuit currents are also taken into account in the analysis. The model is compared to HSPICE simulations and other previously published works for different submicron technologies reporting very high accuracy. The model presents a simple way to compute the crosstalk induced delay bounds showing an excellent accuracy with respect HSPICE simulations. The fully analytical description of the delay allows a quick estimation of this magnitude since no numerical analysis is required. This provides a model that can be incorporated in CAD tools and provide a quick estimation of the delay. The model is also useful to investigate the impact of design parameters on the delay.

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