Nanometer Design: What are the Requirements for Manufacturing Test?

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Why is nanometer technology different from any other previous smaller geometry process? Why should the requirements for manufacturing test be dissimilar to what we have had until now? In the past, most test challenges paralleled the device transistor count and Moore's Law of device complexity was a good predictor of their magnitude.

Nanometer technology is affecting test in several new significant ways. Complex copper interconnects, low-k dielectric materials, continued transistor scaling, and new manufacturing processes are completely changing defect distributions. There are more node-to-node bridges undetected by tests for stuck-at faults, more node-to-node resistive bridges that require at-speed test, more in-line resistances caused by defective vias, and more cross-talk effects undetected by Iddq tests. Numerous small delay defects are detected only when they propagate to outputs with a small slack.

In addition to traditional defects, in nanometer technology, circuits often malfunction as a result of design and process marginalities that increase delay sensitivity, noise sensitivity and manifest themselves as cross talk and IR drop effects. Even though those are not the traditional defects these types of malfunctions have to be detected and diagnosed through test techniques. The transistor scaling rules that define optimal performance require that, with reduced transistor gate length, both the voltage and gate oxide are reduced as well. That in turn increases leakage current and diminishes effectiveness of Iddq test. More fragile transistors also impose restrictions on reliability screening such as burn-in test.

Nanometer technology enables manufacturing of very large SoC designs that have many cores originating from a variety of sources. The challenge here is to integrate different test solutions provided by suppliers of those cores into one comprehensive chip level test. Even though the designs are bigger and more difficult to test, one of the principal requirements is to reduce the cost of manufacturing test.

This panel, comprised of the industry experts, will debate the requirements for manufacturing test for nanometer technology designs. In particular, the panel will address the following topics.

- What are the requirements for high quality test?
- New types of defects that should be targeted.
- Most significant design and process marginalities.
- The biggest new constraints impacting test.
- Requirements for new DFT methodologies supporting high-quality low-cost manufacturing test.
- Other requirements for efficient manufacturing test.
- Requirements for reliability screening.
- Test integration and productivity requirements.
- Test requirements to support silicon debug and in-production diagnostics.

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Moderator: Dr. Janusz Rajski, Chief Scientist and Director of DFT Engineering, Mentor Graphics Corp.

Panelists:
Peter Muhmenthaler, Infineon Technologies (D)
Eric Haioun, Motorola SPS (F)
Erik Jan Marinissen, Philips Research (NL)
Richard Illman, Cadence Design Foundry (UK)
Ben Bennetts, Bennetts Associates (UK)
Shane Dowd, Jennic Ltd (UK)
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Industry Expert views

Over the years, industry experts have articulated a variety of views where they have some measure of common ground in some key areas while having diverse positions on others. The experts forming this panel are representative of the industry in terms of the depth of experience and quality of technical perspective. The panel will be a forum for a stimulated discussion on the driving forces in the industry regarding design for test. These are formative times as we take on the challenges raised by the demands of the newer technologies.

We will hear a more detailed presentation of positions during the panel discussion but here are position statements from some members of the panel.

Richard Illman

Cadence Design Foundry

The real challenges for 90nm in are likely to lie in the area of DFT rather than manufacturing test. The move to 90nm technology and beyond introduces significant changes in the "back-end" design process. This is due to several reasons:

- The delays are "wire dominated" rather than "gate dominated", consequently the synthesis process must be "layout oriented" to achieve accurate timing results. "Wire load" models can no longer be relied upon.

- "IR-drop" and cross-talk effects add additional complexity to the timing verification.

- More computationally expensive algorithms, using "2.5D" are required to extract accurate parasitic capacitance data.

Other features of large SoC designs that affect DFT/ATPG include:

- The use of IP blocks from external suppliers.
- Increased numbers of clock domains
- Use of memories with built-in redundancy/repair

Conventional DFT approaches cause the chip to operate in a manner that is significantly different from the functional mode of operation:

- More simultaneous switching of internal clocks
- Higher "switching activity" than in functional operation

As issues such as IR-drop and cross talk become more significant this gives a fundamental problem. Do we design the chip to operate correctly under test conditions but which is then "over-designed" for normal functional operation? Alternatively do we design for functional operation and tolerate fails in test mode due to these marginal effects?

The gap between the costs of DFT/ATPG and the "place and route" activities appears to be increasing. Typically the man-power costs are 5~10 times greater for P&R than for DFT and the cpu time consumed is between 10x and 100x greater.

As a result of these two trends the emphasis on DFT/ATPG will be to minimise the impact of the DFT on the physical design process and the operation of the device. This will take several forms, including:

- Test logic insertion will tightly integrated into the overall synthesis flow rather than being a "stand-alone" process.

- Increased sequential depth algorithms will be used to avoid the use need for single synchronous clocks in test mode. The clock operation in test mode will be very similar to the operation in functional mode.

- Techniques for reducing switching activity during scan "shift" and "capture" operations

- Increased use of "vectorless sign-off" methodologies allowing designs to be sent to fabrication before completing ATPG.

Overall, the new emphasis will be on minimising the impact of DFT/ATPG on the design flow and using more sophisticated DFT checking/ATPG algorithms to solve the problems. Where new test logic is added e.g. for test data compression, the key requirement will be to minimise the impact on the functional logic within the design.

Ben Bennetts

Bennetts Associates

I would like to make three basic but related points:

1. We have been mesmerised by fault models and their relationship, or otherwise, to manufacturing defects for far too long. Fault models, such as the classic stuck-ats, wired-AND/wired-OR bridging and now transition and path delay fault models should **not** be viewed as simulation images for the effect of manufacturing defects on the behaviour of a logic circuit. They are simply a means to an end – that is, a way for an automatic pattern generator to derive tests that exercise a certain path through a logic circuit. If you go back to Eldred's 1959 JACM paper, you will find no mention of the stuck-at fault model. The thesis of his paper was "exercise all possible structural paths through the circuit.." In 1959, this was revolutionary thinking given that upto that time, most testing of electronic products was done by visual inspection followed by functional exercise.

So, let's stop dreaming up yet more fault models to match predicted nanometer defects. Let's instead go back to basics and reset the structural metric back to "how many structural paths exist, how many should we exercise, and how many have we exercised?"

2. Traditionally, we think about device test objectives in two fundamentally different ways – functional test ("Does it do what it is supposed to do at the right time?") and structural test ("Are there any unwanted manufacturing defects?"). We can add refinements to both these very loose definitions e.g. a broad functional objective can become a narrower application-mode-only objective, or a structural objective can be qualified by defining an acceptable level of manufacturing defects consistent with the product and its market. But in general, we can only measure success in the structural domain – the highly suspect fault-cover metric. There is no realistic metric for functional test. A major challenge as we dig deeper into nanometer technology is to determine a meaningful metric for functional test i.e. we have to answer the question "How much functional test is enough and how are the tests generated?"

3. Once we have more meaningful functional and structural metrics, then we can begin to think more about the impact on DFT: the objectives, the metrics, and the enabling technology of tools and flows. Essentially, DFT needs to split into two related DFTs: Design-For-Structural-Test (DFST) and Design-For-Functional-Test (DFFT). But, both approaches should be pegged more closely to the quality requirements of the device, especially escape rates (false passes). Plus, we have to be able to carry out trade-off analyses between the two approaches.

In addition, more thought needs to be given to DFT from a diagnostic point of view rather than just concentrate on DFT for detection.

Food for thought?

Eric Haioun

Motorola SPS

There are some key areas where designers are focused on for the next generation nanometer designs.

In my view, I see the following as important areas, which are driving the industry to seek robust solutions:

- At speed testing:
  - Path Delay fault coverage for most critical paths
  - Path Delay fault coverage for paths to / from memory
  - Improve run time with user-defined capture procedures
- Low cost tester (with pin sharing, compression, etc…)
- Memory issues, interface with Scan
- Managing huge chips (>100M transitors) with low cost ressources (Linux 32bits -> 64bits)
- Rapid prototyping, early detection of DFT issues
- Manage Flexible Scan architectures

Shane Dowd

Jennic Ltd

Comments centred on Moore's law probably still hold true in terms of the raw magnitude of potential test data delivered with large devices using traditional structured DFT techniques. The search for new defect types and fault manifestations require inclusion of additional testing techniques to augment standard deliveries. The importance of delay and transition fault testing will rise in dominance for digital testing to a point where the stuck-at-model will only be used as a basic functional confidence measure.

Iddq testing will still be a dominant requirement, albeit with new techniques to improve its effectiveness. I'm not at all sure about the comment regarding 'cross-talk effects undetected by Iddq tests'? Iddq tests by very nature are a static form of test and could not detect cross-talk effects. Isolated power islands on a single device will, without doubt, be one area where increased effectiveness of Iddq tests can be addressed. In terms of test time issues on Iddq, I suspect that more capable PMU's will become mainstream on ATE, without the need for restart and calibration between measures, coupled with shorter measurement times.

The concept of core testing and integration of test from various sources is going to be a huge challenge – I suspect the large chip makers will resort to removal and refit of test to avoid the challenge of non-compatible structure and date integration. The challenge of reducing manufacturing test cost will always be dominant. Improvements in test application strategies (multiple cores at once), multiple like cores treated as a single core for testing, reuse of core ATPG data at device level etc.

In terms of debug and analysis the industry is already very much aware of memory issues, soft errors, redundancy, repair etc, yet we are still not at the point where we are willing to apply these techniques to logic cores. I suspect redundancy of critical logic blocks will become more prevalent in the future with on-chip test and configuration during manufacture test.

The future of large chip design will continue to build on the already high percentage of mixed signal content. Test cost is a major issue for mixed signal testing – the aim for low cost ATE and reduced test time will drive new techniques for handling the mixed signal issue. Designers will be forced into pessimistic design at w/c corners. Thin ox brings new issues for gate capacitance and will make noise more of an issue, and this is before we try to design at less then 1V vdd. Via resistance has huge variation and is prone to defects on smaller processes. Will it be possible to complete mixed signal test using standard digital testers? Advances in board design using precision DAC's and ADC's may well help, together with movement of the stimulation and measurements equipment to on-die. These techniques will have reduced accuracy over full mixed signal test and will be prone to the noisy digital test environment. Trade-offs will be centred on the absolute cost of test against the quality requirements of the end component.

Points to consider

Who is responsible for test? The concept of structured DFT is still not really hitting home with design teams. DFT is still a retrofit activity (post design) – cannot continue the design process in this manner.

- Cost of test – intrinsic to value/quality of test requirements.

- Mixed signal content – characterisation/manufacturing test, is there a difference? New methods for reducing mixed signal test cost will appear

- Low cost ATE – is this a viable way forward. A huge portion of test cost for large devices is and will be ATE related. The future of low cost ATE will dominate high volume consumer products (but how?)

- Physical effects – process defects at 90nm and below will reveal new fault structures that will require detection. Is it time that ATPG engines were brought into the physical world – layout aware ATPG is an area of test generation and diagnosis that needs to be addressed.

- Core integration and test reuse is not so much an issue at present however below 90nm it may well become a must for design productivity. This requires standardisation across the industry to encourage mass adoption of test reuse.

Where should we worry about manufacture tests? At wafer probe or final assembly test? Packaging and assembly costs are extending to a point where the raw die

is only a fraction of the final procurement cost. Wafer level test access mechanisms must be addressed to ensure known-good-die feed the assemble process.

CAE enabling techniques – scan chain re-ordering as an example was great at solving the metal congestion issues up to 0.18micron technologies. Still useful for metal congestion issues but nearest neighbour rules play havoc on timing issues for large devices. Scan chain re-ordering must now take on board clock skew, re-timing partitioning, false-paths etc.

What is a false_path? Does not exist in terms of ATPG, or should we only target functional faults. When do we know when to stop testing? Should we target functional faults at all, or simply concentrate on searching for defect spreads on a die, simple techniques could be used to find devices with defects, but does that defect mean a functional failure or a part waiting to fail in the field?

Erik Jan Marinissen

Philips Research Laboratories

The challenge of test development for integrated circuits is to find the right trade-off between *Good*, *Cheap*, and *Fast*: manufacturing tests that deliver good quality for low costs, and which can be developed in a short period of time. This challenge has been in place ever since we make ICs, and will remain with us into the future. The right trade-off point depends strongly on the application domain of the IC. For example: it is obvious that the test quality required of ICs that go into NASA's Space Shuttle is quite different from that of ICs meant for a five-dollar Tamagochy toy. In my understanding, the organizers of this panel have asked to predict how the trade-off point will be influenced by technical changes in manufacturing, design, and test technology.

The progress in semiconductor manufacturing technology enables us to integrate more components of decreasing feature sizes onto a single die. Hence, most test technology challenges stem from the facts that (1) everything gets *smaller*, while at the same time (2) everything gets *bigger*.

Good Testing

Manufacturing defects can be classified as 'shorts' or 'opens'. Traditionally, shorts have dominated the semiconductor defect population. Due to changes in semiconductor manufacturing techniques and higher operational frequencies, the relative importance of opens is growing.

Severe (low-ohmic) shorts can easily be detected by stuck-at and delay-fault tests. The detection capability of current-based I_{DDQ} testing for shorts goes further, such that more subtle shorts of, say, 10 kΩ, still get detected [1]. The increase in level and variance of the leakage currents for smaller processing dimensions threatens current-based testing and its superior detection qualities for shorts. Fortunately, innovative research has so far kept current-based testing alive by creating advanced versions of it. "I_{DDQ} testing is like oil reserves. We hear it is going to die, but every time its life gets extended by innovative research." [2]

Severe (high-ohmic) opens up till, say, 5 MΩ can relatively easy be detected with stuck-at tests. More subtle opens up till, say, 100 kΩ require the advanced detection capabilities of delay-fault testing [1].

Trends in improving test quality are the following.

- Increasingly, there is no single fixed threshold to decide on pass/fail of a device. In I_{DDQ} testing, for example, the maximum operational frequency of the IC (determined by means of on-chip ring oscillators) needs to be correlated to the current measurements for a balanced judgement [1]. Another example is testing in which the pass/fail decision is not taken for one individual device, but based on *outlier behavior* for a larger population (wafer, batch) of ICs [3].
- Increasingly, manufacturing testing serves not only as a means to separate bad from good parts, but also to provide relevant feedback in order to improve design, manufacturing, and test processes. Analysis of defects in well-organized feedback loops has revealed that many spot defects are not at all random in nature, but have systematic, structural causes. Finding those causes is key in improving yield and product quality [4].
- We start to see the first serious impacts of soft errors, i.e., temporal glitches caused by alpha particles and neutrons [5]. Soft errors cannot be tested for in the factory, and the only known protection technology is by means of masking: fault tolerance. Traditionally, testing and fault tolerance do not go together very well, simply because detection and masking are contradictive. I predict an increasing role for fault tolerance, not only in memories, but also in digital logic. Fine-grained fault tolerance might relieve hard-to-meet test quality constraints, although masking of

hard defects will deteriorate the protection offered against soft errors [6]. Test technology and fault tolerance will have to learn to live together in a new equilibrium.

Cheap Testing

The price of an ATE depends on its channel count, vector memory depth, and accuracy. Companies have started to realize that for many of their (structural) tests, they use at most 10% of the capabilities of their expensive ATEs [7]. This led to a wave of interest into low-cost *'DfT Testers'*. Such testers do work, provided that one is willing to rely on DfT-based structural testing only, and is willing to add some on-chip DfT hardware to compensate for the reduced capabilities of the low-cost ATE.

- Low-channel-count testers can be used if complemented with Reduced Pin-Count Testing (RPCT) hardware on chip [8]. Alternatively, RPCT allows to test multiple ICs in parallel on the same ATE ('multi-site testing'), such that the ATE base costs can be amortized over multiple devices.
- Most test cost reduction techniques focus on reducing the required test vector memory depth and/or associated test application time. For many years, Built-In Self Test (BIST) was seen as the only solution. Many companies have indeed adopted BIST for embedded memories as a mainstream DfT approach, while the adoption of BIST for logic is a lot less. The area costs of generating a good set of logic stimuli on-chip can typically only be justified if the BIST capability needs to be reused as system or field test. Fortunately, many test data compression schemes are available nowadays. These techniques exploit the fact that ATPG test patterns contain a large fraction of don't care bits. For relative low area expenses, the test data volume is reduced tenfold or more, which provides sufficient breading space for now [9].
- Accurate pin electronics will remain necessary and expensive. The gaps between IC and ATE operating frequencies and the associated required accuracies will continue to grow. Fortunately, we do not need high accuracy on all ATE channels. One or a few high-accuracy channels, combined with many low-cost low-accuracy channels will do too.

Fast Test Development

The larger the IC, the more attractive a modular test approach. Non-logic modules (e.g., memories, analog, RF) and black-boxed third-party cores require stand-alone testing. However, modular testing also reduces the test generation time, as it presents more digestable chunks of circuitry to our ATPG tools and enables concurrent engineering. At the same time, modular testing facilitates test reuse, which especially pays off in the case of a family of chip derivatives [10].

Modular testing requires an on-chip test infrastructure in the form of wrappers and Test Access Mechanisms (TAMs). With the endorsement of IEEE 1500 SECT [11] as a full standard around the corner, I predict an increased attention for modular testing. Hopefully, the adoption of the standard will also stimulate EDA vendors in the further development of tools in this domain.

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