Synthesized Compact Models (SCM) of Substrate Noise Coupling Analysis and Synthesis in Mixed-Signal ICs

Hai Lan and Robert Dutton
Stanford University
Department of Electrical Engineering
CISX-305, Stanford, CA 94305, U.S.A.
{hailan, rdutton}@gloworm.stanford.edu

Abstract

An approach for synthesized compact models (SCM) of substrate noise coupling is presented. The model is formulated using parameterized and scalable Z matrix. The improvement in modeling near field effects results in better substrate noise modeling for analog circuits. The geometrical scalability of the model provides a bi-directional link between noise analysis in the post-layout phase for verification and the noise-aware layout synthesis using convex optimization techniques. The model is validated by rigorous EM and device simulations. Several application examples are used to demonstrate the bi-directional usage of the model.

1. Introduction

Noise coupling through the lossy silicon substrate has been a severe problem, preventing the integration of sensitive analog and RF circuits with noisy digital circuits on the same die. This continues to be an even more critical factor in the deep submicron era, limiting the performance of the mixed-signal applications and the trend toward System-On-Chip (SOC) integration. Consequently, there has been considerable research on characterizing and modeling the substrate for noise coupling analysis. Most reported techniques resort to numerical algorithms that solve the device- or electromagnetic-level equations, e.g., Poisson and continuity equations, quasi-static Laplace equation or full-wave Maxwell equations. These methods in general are based on fine grid meshing schemes and solve the discretized partial differential or integral equations and therefore can be very accurate [1] [2] [3]. But they are normally computationally very intensive, which limits their application to substrate noise analysis for simple configurations rather than practical application of full-chip substrate noise analysis. Moreover, due to the meshing requirements, these methods can only do noise analysis and are not very insightful in providing the mixed-signal IC designer with direct layout synthesis guidelines for noise-aware layout floor planning.

In order to perform both substrate noise analysis and noise-aware design, synthesized compact models (SCM) are developed in this work. This paper is organized as follows. The SCM formulation and methodologies are given in Section 2, where improvements in modeling the near field effects are discussed. Substrate noise-aware synthesis based on scalability of the SCM and its formulation that exploits the convex optimization technique are discussed in Section 3. Applications of the SCM are demonstrated in Section 4 to show the both computation efficiency and bidirectional usage in linking behavior and layout. Finally, conclusions are drawn in Section 5.

2. Synthesized Compact Models (SCM) formulation and verification

2.1. Z matrix based generic scalable model

It has been shown in [4] that the two port network resistance-based scalable model cannot be directly extended to multiple contact configurations due to the influence from neighboring contacts. For a multiple contact configuration, which represents the real situation in practical circuit layouts, multi-port Z matrix based models can reasonably predict the overall interaction between any two contacts in the presence of all other nearby contacts. In general for an N contact configuration, the corresponding Z matrix characterizing coupling between two contacts is:

$$[Z] = \begin{bmatrix} . & . & . & . & . \\ . & Z_{ii} & . & Z_{ij} & . \\ . & . & . & . & . \\ . & Z_{ji} & . & Z_{jj} & . \\ . & . & . & . & . \end{bmatrix} \quad (1)$$

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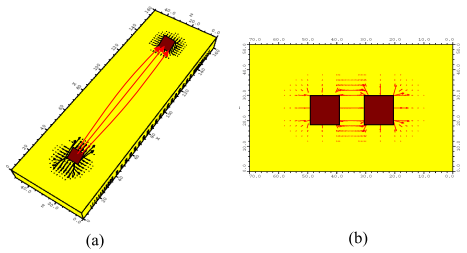


(a) (b)

Figure 1. (a)Far field region: point to point lumping of elements. (b)Near field region: more spreading resistance effects essential.

where all the self- and mutual-impedance terms in the Z matrix have been modeled by the geometry-dependent analytical expressions in [5].

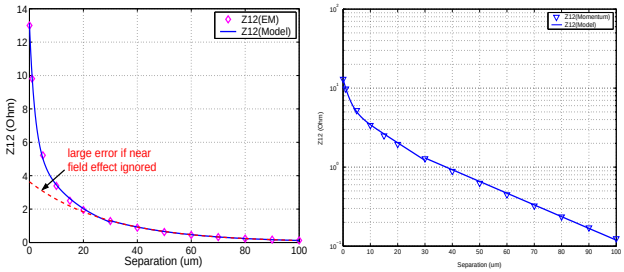
2.2. Far field and near field implications

Depending on the relative aspect ratio of the size of two contacts and the separation between them, the near field effect becomes more significant due to the spreading resistance effects of the current flow when contacts are close to each other. When the separation is relatively large compared to the contact size itself, the far field effect dominates, which mainly depends on the separation. However, when two contacts are close to each other, both the separation and the perimeter affects the strength of coupling, as shown in Figure 1.

Properly differentiating and modeling the near field and far field effects is critically important in guard ring structure analysis. Moreover, two regions also helps to reduce the overall complexity of the substrate network and allows hierarchical modeling to be used [6]. Although the scalable model developed in [5] is generally good for far field situations, it shows relatively large errors when the near field effects become more prominent, as shown in Figure 2(a). Rigorous electromagnetic (EM) simulation using Momentum [7] was performed to get the mutual coupling term Z_{12} between two identical contacts with size of $20\mu m$ by $20\mu m$. As can be seen from the comparison in the figure, the model proposed in [5] agrees well with Momentum simulation result in the far field region while in the near field region it underestimates the mutual coupling. Thus, it is necessary to develop a more comprehensive model, including both near- and far-field effects.

2.3. Improved Z matrix based SCM

Rigorous EM and 3D device level simulations reveal that the self impedance term Z_{ii} in the Z matrix is a contact



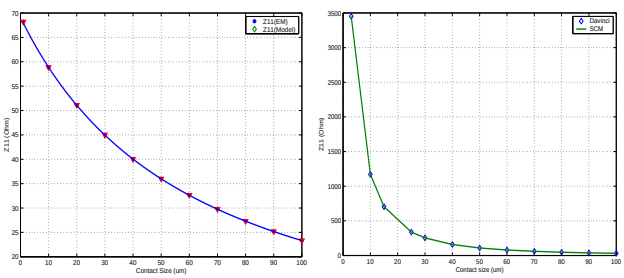
(a) (b)

Figure 2. (a)Comparison between Momentum and model in [5] shows that ignoring near field effect results in large deviation. (b)Log scale plot shows that in the near field region Z_{12} decays faster than exponentially.

geometry-dependent function. The self term Z_{ii} can be modeled by the following analytical expression:

$$Z_{ii} = \frac{1}{k_1 area + k_2 perimeter + k_3} \quad (2)$$

where k_1,k_2 and k_3 are fitting parameters, which are only process-dependent. Figure 3(a) shows both Momentum simulation results and model predictions of Z_{11} for a heavily doped substrate with lightly doped epitaxial layer process. Figure 3(b) shows both Davinci simulation results and model predictions of Z_{11} for a lightly doped substrate.



(a) (b)

Figure 3. (a)Comparison of Z_{11} between SCM and Momentum simulation for heavily doped substrate with epitaxial layer. (b)Comparison of Z_{11} between SCM model and Davinci simulation for lightly doped substrate.

For the heavily doped substrate with a lightly doped epitaxial layer the heavily doped substrate acts as a current sink node and the lightly doped epitaxial layer is thin. Hence the near field effect only shows significance when the separation between two contacts is much less than the thickness of the epitaxial layer. As the separation increases, the coupling decays in an exponential fashion in the far field region

and faster than exponential in the near field region, as shown in Figure 2(b). A complete model of Z_{ij} is proposed here to account for both near and far field effects:

$$Z_{ij} = \begin{cases} Z_0 e^{-\beta x} & \text{far field} \\ Z_{01} e^{-\gamma_1 x_1} + Z_{02} e^{-\gamma_2 x_2} & \text{near field} \end{cases} \quad (3)$$

where β,γ_1 and γ_2 are process dependent fitting parameters. Z_0, Z_{01} and Z_{02} can be derived using the self impedance formula of the SCM.

In lightly doped silicon substrates, the near field effect still exists but exhibits its effects in a slightly different way. For the far field configuration the current injected into the substrate by the noise aggressor tends to penetrate more deeply in the vertical direction before it is sensed by the victim while for a near field configuration it tends to crowd to the surface region along the direct path between two contacts. As separation increases, the coupling decays in a linear fashion in the far field region but faster than linear in the near field region. Thus it is modeled as follows:

$$R_{ij} = \frac{\alpha d_{gmd}^{p}}{\sqrt{area_i} + \sqrt{area_j}} \quad (4)$$

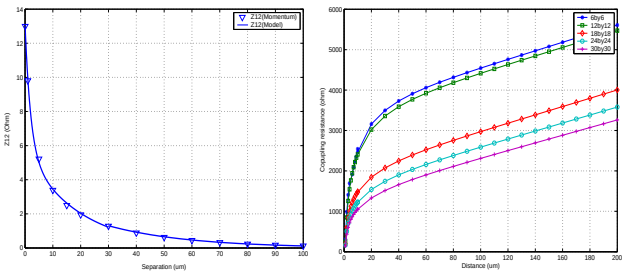
where d_{gmd} is defined as the geometric mean distance between the two contacts and α and p are process dependent fitting parameters. Note that the geometric mean distance implies a linear decay in the far field region and faster than linear decay in near field region.

Figure 4(a) shows the comparison of Z_{12} between the SCM model prediction and Momentum simulation results for a heavily doped substrate with epitaxial layer. The model agrees with Momentum simulation results in both near and far field region. Figure 4(b) shows the comparison of the coupling resistance R_{12} from SCM model predictions and Davinci [8] simulation results for different shapes of contacts in lightly doped substrates.

3. Substrate noise aware layout synthesis

The substrate model discussed above is formulated using a set of analytical expressions with a few fitting parameters. The fitting parameters can be extracted from rigorous EM or device simulations and can be further calibrated from on-chip probing experiments with representative contact configurations for a given process. Once the fitting parameters are obtained, the substrate noise coupling between any two contacts can be easily computed using the Z matrix macro model obtained. Meanwhile, the equivalent circuit model can be readily extracted from the Z matrix so that it can be included in standard circuit simulators to perform noise coupling analysis.

Since the proposed model does not require meshing and is geometry and spacing dependent for a given process, it is possible to use this model to support circuit layout optimization and synthesis, and noise-aware floor planning. A typical application, given the signature of the digital noise injected into the substrate and the maximum amount of noise tolerable, is to determine the optimal distance between the noisy block and sensitive blocks.



(a) (b)

Figure 4. (a)Comparison of Z_{12} between SCM and Momentum simulation result in heavily doped substrate with epitaxial layer process.(b)R_{12} as a function of separation for contacts with different shapes in lightly doped process.

Owing to its parametrization and scalability with geometry, SCMs provide the key of bi-directional connection between substrate noise analysis and substrate noise-aware layout synthesis. The layout optimization and synthesis problems can each be formulated as a constrained convex optimization problem as follows:

$$\text{minimize} f_0(x) = e^T x$$

$$\text{subject to} \begin{cases} x_i > 0, i = 1, 2, ...q \\ f_i(x) = \frac{Z_i(x) I}{N_{imax}} \leq 1, & i = 1, 2, ...m \\ h_i(x) = \frac{area_i}{area_{imax}} \leq 1, & i = 1, 2, ...l \\ g_i(x) = \frac{area_i}{area_{imax}} = 1, & i = 1, 2, ...p \end{cases}$$

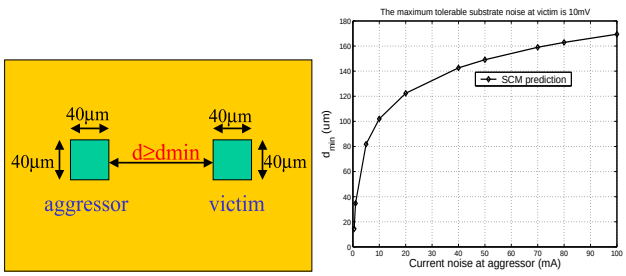
where the optimization variable set is:

$$x = \begin{bmatrix} area_1 \\ perimeter_1 \\ . \\ . \\ area_n \\ perimeter_n \\ d_{1,2} \\ . \\ . \\ d_{n-1,n} \end{bmatrix} \in R^k \quad k = \frac{n^2+3n}{2} \quad (5)$$

In the formulation, the vector $I \in R^n$ denotes the digital noise signature from multiple noisy circuit blocks and Z_i is the ith row vector of Z. Vector $f_i(x)$ represents m sensitive blocks with a maximum tolerable substrate noise. Vector $h_i(x)$ denotes the contacts which have the maximum

area constraints and $g_i(x)$ denotes the contacts which have assigned fixed areas. Once the problem is formulated in canonical form for convex optimization, there is a single global optimal solution. The problem can be very efficiently solved using interior point methods [9]. Given the noise injection signature at the aggressor side and the maximum substrate noise tolerable at the victim side, the SCM is then used to determine the key layout geometry parameters, for example, the minimum distance between two circuit blocks and the spacing of the guard ring structure for area-efficient noise isolation.

Figure 5 illustrates a simple application of noise-aware design. Figure 5(a) shows a layout of two contacts in a heavily doped substrate with an epitaxial substrate; the backplane is intentionally left floating to emphasize the substrate noise coupling. In the layout there is one noise aggressor contact and one noise victim contact with dimensions as shown in the figure. The critical design parameter here is the distance between them. If the maximum noise disturbance tolerable to the victim is fixed, then the required minimum separation is a function of the strength of the current noise at the aggressor side. Figure 5(b) shows the design tradeoff curve between the minimum separation needed and the noise current at the aggressor.



(a) (b)

Figure 5. (a)Critical design parameter d_{min} (b)Design tradeoff curve of d_{min} and aggressor noise.

4. Application examples

4.1. Substrate model generation using SCM

An example of a simplified latch circuit in a BiCMOS process is considered here to show the effectiveness of computing substrate resistance using the SCM approach. Figure 6 shows the abstracted layout of a BiCMOS latch circuit with the presence of a CMOS inverter located some distance d away. A five-port substrate network is generated after grouping the nearby contacts. Since the N-well capacitance and the BJT collector junction capacitance can be

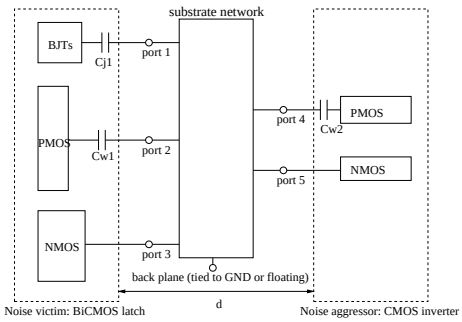


Figure 6. Example in 4.1. Floor plan assumed to extract the substrate model for a BiCMOS latch circuit and a CMOS inverter.

separately and locally computed, the network shown here only represents the coupling resistance due to the substrate and it can be connected to the well- and junction- capacitances for complete simulation. The substrate network is extracted from 3D Davinci simulations and also computed using the SCM discussed above for various separation d between the latch circuit and the noisy inverter. Selected resistance values in the substrate network are tabulated in Table 1. SCM shows reasonable accuracy compared to Davinci simulation results in all cases. The computation cost is also shown in Table 2.

4.2. Noise-aware floor planning

Figure 7 shows an example based on an abstracted version of the mixed-signal circuit layout in [10]. In the layout, there are two sensitive analog circuit blocks with multiple digital noise sources from LN1, LN2, and REF respectively. Given the noise signature of each noise aggressor and the sensitivity of each victim block, determining the optimal spacing parameters between each aggressor and victim, namely, d_1,d_2,d_3,d_4,d_5 and d_6, is formulated as a convex optimization with the SCM developed for a lightly doped process, where $Na = 3.9 \times 10^{16} cm^{-3}$. The constraint set is specified in a customized format as $(I_1, I_2, I_3, V_{sub4}, V_{sub5})$, where $I_{1,2,3}$ are the noise current from aggressor 1,2,or 3 and $V_{sub4,5}$ are the maximum tolerable noise to victim 4 or 5. The sensitive circuit blocks 4 and 5 are assumed to tolerate a maximum substrate noise of 10mV. Several different constraint conditions, i.e., different strength of digital noise from the aggressors, are used in the experiment.

Table 3 summarizes the layout parameters $d1 \sim d6$ automatically synthesized based on the SCM using convex optimization. It can be seen from the synthesis result that the optimal spacing parameters are obtained in order to guide the circuit block level floor planning. When the current

Table 1. Selected resistance values of example in 4.1. All resistances are in Ohms

Separation	*Method*	$R_{1,0}$	$R_{3,0}$	$R_{1,4}$	$R_{1,5}$	$R_{2,4}$	$R_{2,5}$	$R_{3,4}$	$R_{3,5}$
d=2 μm	SCM	3.77K	2.18K	229.08K	2.40M	11.28K	22.25K	146.17K	51.00K
	Davinci	3.26K	1.99K	240.13K	2.68M	11.96K	23.81K	150.36K	53.86K
d=5 μm	SCM	3.78K	2.15K	257.03K	2.65M	21.69K	46.26K	157.90K	63.87K
	Davinci	3.50K	1.94K	265.76K	2.88M	23.45K	49.73K	161.80K	66.85K
d=30 μm	SCM	3.68K	1.85K	3.78M	17.66M	932.49K	2.05M	1.27M	1.13M
	Davinci	3.30K	1.76K	3.85M	18.54M	990.11K	2.45M	1.50M	1.44M
d=100 μm	SCM	3.66K	1.80K	577.67M	922.72M	406.07M	633.35M	258.26M	395.99M
	Davinci	3.29K	1.69K	600.54K	990.16M	470.28K	684.44M	290.17M	440.02K

Table 2. Comparison of computation cost in example 4.1(for $d = 100\mu m$ case)

	Time (sec)	Grid used	Platform
SCM	1.55[1]	No grid	PC Pentium III 1GHz
Davinci	1549.8	60588	HP 9000/J6000 2 552MHz PA8600 CPUs

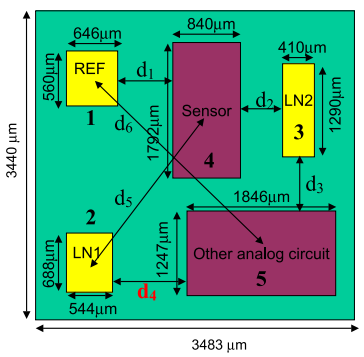


Figure 7. Example in 4.2. Layout floor planning using SCM.

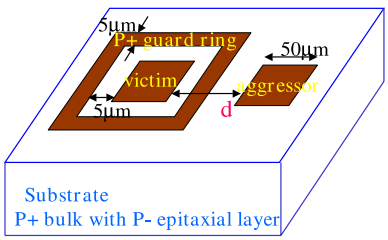


Figure 8. Example in 4.3. A typical P+ type guard ring structure.

noise from block 3 increases from 30mA to 60mA, the spacing parameters d_2 and d_3 have to increase so that the noise sensed by block 4 and 5 is less than their noise margins. Since most noise current from block 3 is absorbed by blocks 4 and 5, the spacing parameters related to blocks 1 or 2 remain the same. When the noise current from blocks 1 and 3 simultaneously increase, one has to increase the spacing parameters d_1,d_2,d_3 and d_6 in order to ensure that the substrate noise affecting blocks 4 and 5 are within their noise tolerances. The SCM using the convex optimization automatically gives the optimal layout parameters, which helps circuit designers to determine a layout floor plan, quantitatively based on substrate noise.

4.3. Guard ring structure

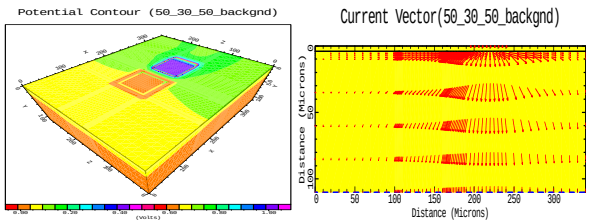
Figure 8 shows a typical P+ guard ring structure used to reduce the substrate noise impaction of the aggressor on a victim block for a heavily doped process. Both Davinci simulation and SCM are used to extract the effective coupling resistance R_{eff} between the aggressor and victim when $d = 30\mu m$.

A total of $47,043$ grid points were used in Davinci simulations and the computation time was 201 seconds. Figure 9(a) shows the voltage potential contours and (b) shows the cross sectional view of the current flow line vectors. As can be seen from the Davinci simulation results, most noise current is removed by the back plane of the heavily doped substrate. The effective resistance extracted from Davinci is 306.1Ω.

In SCM computation, first a direct circuit model is generated as shown in Figure 10(a). Some resistances can be lumped. Figure 10(b)shows the general lumped equivalent circuit model of the guard ring structure, which is a 4-port resistance network. The 4th port denotes the back plane in epi process, which is normally tied to GND. In some practical situations the back plane has to be left floating, e.g., when it is used for thermal conduction. It should be pointed out that this generic model is well suited for a variety of biasing, guard ring topologies and back plane configurations.

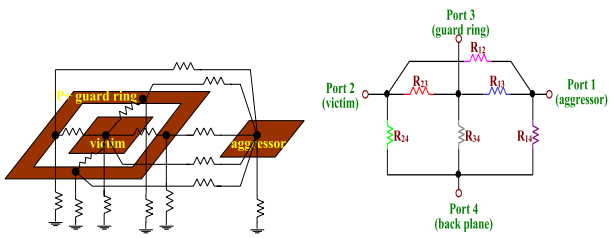
Table 3. Optimal spacing parameters obtained from layout synthesis using SCM (Example 4.2)

constraint set	$d_1(\mu m)$	$d_2(\mu m)$	$d_3(\mu m)$	$d_4(\mu m)$	$d_5(\mu m)$	$d_6(\mu m)$
(10mA,10mA,30mA,10mV,10mV)	97	128	118	89	97	89
(10mA,10mA,60mA,10mV,10mV)	97	149	139	89	97	89
(40mA,10mA,60mA,10mV,10mV)	138	149	139	89	97	130



(a) (b)

Figure 9. Davinci simulation of the guard ring. (a)Potential contour (b)current flow vector.



(a) (b)

Figure 10. (a)Direct circuit modeling of the guard ring using SCM. (b)Generic lumped equivalent circuit model.

In this case, the guard ring and back plane are assumed to be ideally grounded. Then the effective resistance R_{eff} can be obtained by computing the equivalent resistance as follows:

$$R_{eff} = \frac{(R_{12} + R_{23}//R_{24}) \times (R_{23}//R_{24})}{R_{12} + R_{23}//R_{24} + R_{13}//R_{14}} \qquad (6)$$

The SCM required only 0.5 seconds of computation time and the effective resistance is 346.7Ω. In comparing with Davinci based extraction, the SCM is 400 times faster and still achieves a good estimation of substrate noise coupling.

5. Conclusions

In this paper, synthesized compact models (SCM) have been developed for substrate noise coupling analysis and synthesis. Near field and far field effects are discussed and have been included in the SCM model to improve the accuracy in the near field region. The SCM was validated with rigorous EM and device level simulation results. The SCM has been used for substrate noise-aware layout synthesis by formulating the problem in canonical convex optimization form. The computation efficiency and synthesis capability were demonstrated by several application examples. Future work will be carried out using more complex circuit topologies, targeted for full-chip noise analysis and IP block level noise-aware floor planning.

6. Acknowledgements

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