Design of Sub-10-Picoseconds On-Chip Time Measurement Circuit

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Abstract

The rapid pace of change in IC technology, specifically in speed of operation, demands sophisticated design solutions for IC testing methodologies. Moreover, the current technology of System-on-chip (SOC) makes great demands for testing internal speed accurately as the limitation on accessing internal nodes using I/O pins becomes more difficult. This paper presents two high-resolution time measurement schemes for digital BIST applications, namely: Two-Delay Interpolation Method (TDIM) and Time Amplifier. The two schemes are combined to produce a completely new design for BIST time measurement which offers two main advantages: a low range of timing measurement which has never been achieved before, and a small size of layout occupying 0.2 mm^2 or equivalent to 3020 transistors. These two features are undoubtedly compatible with present high-speed SOC design architectures.

1. Introduction

Internal timing parameters in digital ICs are extremely difficult to measure e.g.: set-up and hold time, jitter specifications etc. The difficulty in measuring timing is due to its magnitude, which is in picoseconds. The current technique of using automatic test equipment (ATE) is no longer an effective instrument to support internal timing measurement since the technology of the device under test improves faster than the technology of the ATE. An alternative mechanism for measuring timing is by implementing BIST time measurement. Previous approaches which have been proposed, for example the counter-based technique, the vernier oscillator, time to voltage converter etc. in general suffer from the following limitations:

i. Minimum timing range.
ii. High area overhead of BIST.
iii. Complex calibration process.
iv. Low resolution of measurement.

These limitations led to the implementation of our new concept in time measurement circuits. In our approaches three major advances have been made. The first is the high-resolution time measurement circuit (TMC). The high-resolution TMC implements two delay interpolation methods in its measurement scheme. This method is simple when compared with a previous design [1] and can measure to very low timing margins of 5ps resolution as proven in Pspice simulation results. A range of measurements from 5ps to 160ps is very useful for measuring internal timing parameters of a circuit. Moreover the range of measurement is expandable by adding more cells.

The second advance is the design of the Time Amplifier circuit. The Time Amplifier circuit [4] is able to stretch small timing intervals perhaps below 5ps to a measurable scale. Sumner [3] used a stretching technique in his TMC design by implementing RC circuits as stretch elements. However the application is only suitable for mixed analog-digital circuits. On the other hand the Time Amplifier is fully digitally operated and consisting of only 32 transistors.

Finally the combination of the two designs; high resolution TMC and Time Amplifier, leads to the creation of a new design of a TMC for digital timing measurement. The combination of the two circuits realizes the measurement of time on a scale that never has been achieved before. The Time Amplifier stretches the small timing interval below 5ps with a consistent gain of 10, and then the high resolution TMC will measure the stretched signal accurately. In general this technique can suitably be applied to any high resolution TMC to improve its range of timing measurement below its minimum resolution. The new TMC design comprises 3020 transistors, occupying an equivalent area of 0.2mm^2 using 0.18 μm process technology, has been fabricated. This structure is considered small compared to the latest design [2] which uses 1200 2-input NAND gates equivalent to 4800 transistors.

The remainder of this paper describes the design of the circuit involved within the measurement process and the results of the simulation. Section 2 highlights the general idea of the new TMC. Sections 3 and 4 describe the design of the high-resolution TMC using two delay line interpolation method. The design of the Time Amplifier circuit is described in section 5 whilst section 6 overviews the design of the new TMC and the calibration strategy. Sections 7 and 8 outline the implementation of the overall scheme using 0.18 μm CMOS process. Finally, section 9 concludes the main findings of the research.

2. Design Implementation

The hardware in the new time measurement circuit comprises two stages, namely, the amplifying stage and

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the time measurement stage. In realising the first stage a circuit is required that can perform amplification of the timing signals, and the circuit must be realised using digital circuit design techniques. The Time Amplifier [4] is a circuit that can stretch small timing margins in the range of few picoseconds to a bigger scale with a linear output response. The next stage of the high-resolution TMC design is used to perform the time measurement operation. The resolution of the TMC should cover the linear output range of the Time Amplifier. From the combination of the circuits as shown in Fig. 1, emerges a new scheme of time measurement in digital ICs. The new scheme can provide two measurement options in one IC package: (a) direct application of the TMC to the test signals whose time interval is to be measured. (b) stretching the input signals by using the Time Amplifier before digitizing the timing interval. These two options correspond to the size of the timing interval that needs to be measured. The following equations summarize the test signals used in each option:

$$T_S = (t_{S2} - t_{S1}) \quad (1)$$

$$T_P = \mathbf{A}.(t_{P2} - t_{P1}) \quad (2)$$

where T_S is the timing interval under direct measurement, T_P is the timing interval of the stretched signal and A is the linear gain of the Time Amplifier circuit.

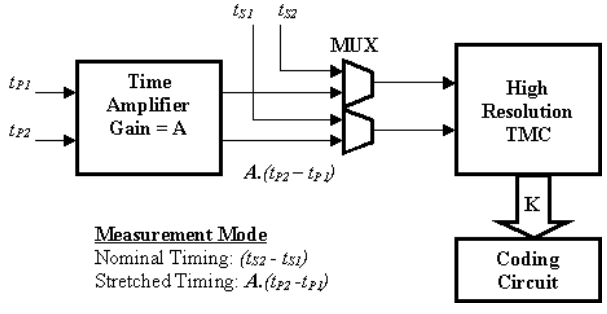

Fig. 1: Block Diagram of the sub-10-ps time measurement circuit

3. High-Resolution TMC

The underlying concept is based on the delay difference between two-delay lines which is known as the two delay interpolation method (TDIM) shown in Fig. 2. This technique has been proposed in [3] for implementing a stabilized time-to-digital converter but the circuit uses bistable elements to digitize the timing interval. This certainly reduces the accuracy of the result when the timing signals tested by the bistable are very close causing metastablility to occur. In our design structure, MUTEXes are used which have ability to filter out metastability. TDIM comprises K cells and each cell consists of two delay elements and a MUTEX. In setting the delay value, two inverter pairs are used. The first inverter pair of the delay element has a structure slightly smaller than the second inverter pair. As a result, the first delay element contributes a delay, Δt, longer than the second delay element. The process of digitizing the interval of two rising signals is started with the faster signal going to the longer delay element. Therefore the first signal will be delayed by Δt, K number of times. Each time the test signals pass through one cell the output is tested to check the result of the difference between the two-inverter pairs. A positive difference will indicate that the first test signal is faster than the second test signal, while a negative difference will define matters the other way round. Eventually the complete result of the measurement is in the form of a thermometer code.

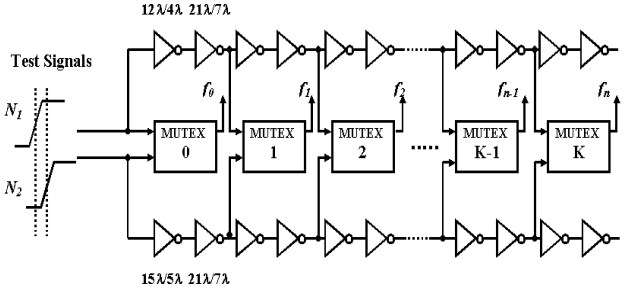

Fig. 2: TDIM delay lines structure

4. 32-Bit TDIM Design

The sizes of 12λ/4λ, 21λ/7λ and 15λ/5λ, 21λ/7λ were used to design the cells of the two delay lines of the TDIM. It has been shown that the pair consistently produces a difference delay of 5ps.

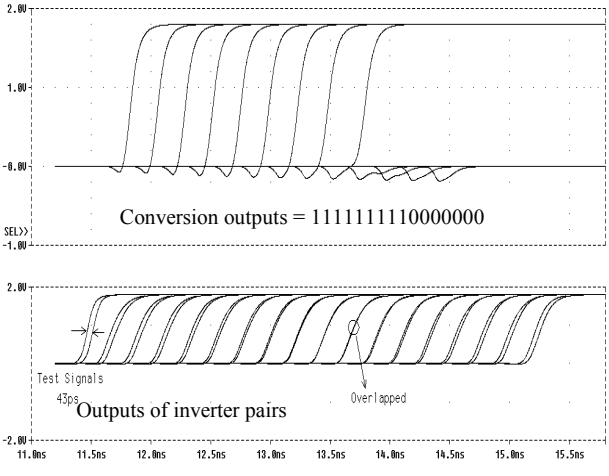

Fig. 3: TDIM simulation result

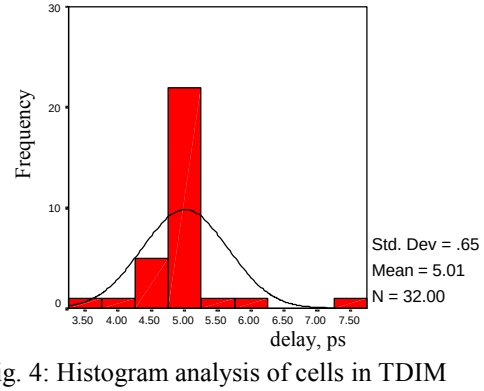

Fig. 4: Histogram analysis of cells in TDIM

Due to the measurement being based on successive operations, the 32-bit output would be in the form of a thermometer code. The completion time of one measurement is equal to the total number of inverters. Hence for 32-bit operation it would be 32 x 2.τ = 64.τ which is equivalent to 3.17ns if the time constant taken for a 0.18 mm CMOS process is 49.6ps (obtained from ring oscillator circuit).

It appears in Fig. 3 that the resolution of 5ps is successfully maintained by each cell. The histogram analysis of Fig. 4 shows a very low standard deviation of 0.65 for the average resolution of 5.01ps.

5. Time Amplifier

The design of the Time Amplifier aims to improve the minimum input range of the TMC. Prior to implementation of the design of the Time Amplifier, three criteria of the amplifier characteristics need to be be analyzed.

i. The linearity of the output response:

It is very important in an amplifier circuit to have a very consistent and linear output response. The basic relationship between input signals and output signals can be formulated as follows:

$$f(out_1, out_2) = A.S(in_1, in_2) \qquad (3)$$

where A is the gain of the Time Amplifier and S is the input signals of the Time Amplifier circuit. In a metastable condition the MUTEX circuit exhibits a linear input output responses over a range of a few picoseconds.

ii. The gain of the Time Amplifier:

The aspect ratios of the transistors are important in setting the gain of the Time Amplifer. The gain can be increased or decreased by properly setting the length and width of the transistors in the MUTEX circuit. In this context the metastability time parameter of the MUTEX was used as a reference. Equation 4 represents the relationships between the metastability time and the size of transistor in the MUTEX circuit.

$$t_m \propto -(L/W).C_{Tot} \ln(\theta.\Delta_t/\Delta_V) \qquad (4)$$

where C_{Tot} is the total capacitance of the internal device and the load , θ is the conversion factor from time to initial voltage at the metastable nodes, Δ_t is the time overlap between the two inputs and Δ_v is the voltage output difference .

The second parameter which could also set the gain of the Time Amplifier is the time offset, t_{offset} of the MUTEX. The time offset is adjustable by making the MUTEX circuit unbalanced [4]. An analysis has been carried out to check the position of t_{offset} when the sizes of the transistors in the MUTEX circuit were altered. Table 1 shows the individual size of the transistors and the results of the t_{offset} in the MUTEX.

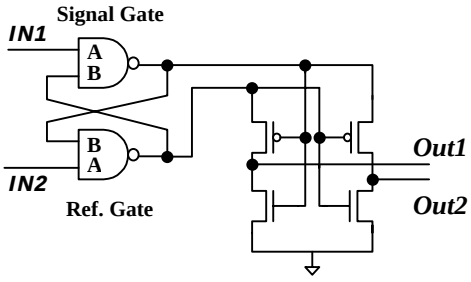

Fig. 5: MUTEX circuit

Tm (ps)	Signal gate transistor width µm				Ref. Gate transistor width, µm				Time offset (ps)
	p	n	p	n	p	n	p	n	
503	6.7	7.5	6.7	7.5	6.7	7.5	6.7	7.5	0
468	6.7	7.5	6.7	7.5	6.7	7.5	8.7	7.5	+1.9
506	6.7	7.5	4.7	7.5	6.7	7.5	6.7	7.5	+1.9
465	6.7	7.5	6.7	7.5	6.7	7.5	6.7	9.8	-5.2
470	6.7	7.5	6.7	5.3	6.7	7.5	6.7	7.5	-4.1
496	6.7	7.5	6.7	5.3	6.7	7.5	6.7	9.8	-9.3

+30 % of normal size -30 % of normal size

Table 1: MUTEX time offset for input range coverage

The longest t_{offset} is obtained when the width of the NMOS transistors in the reference gate and in the signal gate (Fig.5) were set to 30 % greater than the normal size. The t_{offset} is moved to a negative value, -9.3ps (last row in Table 1). The higher the value of the t_{offset} means that the gain is reduced and at the same time the range of timing input interval is increased from 0 to 9.3ps.

iii. The scale of the input range:

The scale should cover a range from below the minimum scale of the TMC. In the TMC, it has been set that the minimum range of the input signal for accurate measurement is 5ps. Therefore the Time Amplifier range should cover the range from its minimum value to slightly overlapping the minimum value of the TMC range at 5ps. Fig. 6 shows the coverage of input range of the Time Amplifier and the TMC. The same technique employed in criterion (ii) directly determines the range of the time scale for the Time Amplifier.

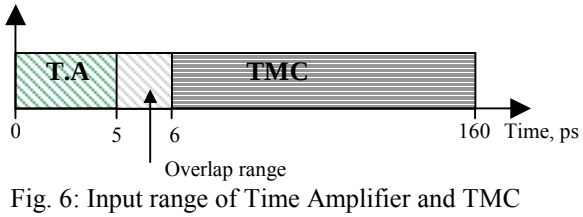

Fig. 6: Input range of Time Amplifier and TMC

The three main criteria described above are extremely important in designing the Time Amplifier circuit using a MUTEX element. However the design of the Time

Amplifier was not a straightforward process. Several designs were proposed and simulated before the circuit shown in Fig. 7 was developed [4]. The time offsets of the two MUTEX circuits were set at different values, one with an offset of + 9.3ps and one with an offset of – 9.3ps. As described in criterion (ii), the time offset will determine the gain and the input range of the input time differences. Therefore, with the proper range between the two opposite offsets, the input time difference, Δ_t, can be set to cover the range ± 6ps as shown in Fig. 6. The time difference of the two outputs, t_{out}, can be calculated [4] by using equation 5:

$$t_{out} = \tau.\ln(t_{offset} + \Delta_t) - \tau.\ln(t_{offset} - \Delta_t) \qquad (5)$$

From equation 5 the gain of the Time Amplifier of Fig. 7 can be derived as follows:

$$\frac{dt_{out}}{d\Delta_t} = -\frac{2\tau}{(t_{offset})} \qquad (6)$$

which yields the calculated gain as 10.14 for the t_{offset}, 9.3ps. The t_{offset}, also sets the output time difference, which is overlapped with the minimum input range of the TMC (5ps – 160ps).

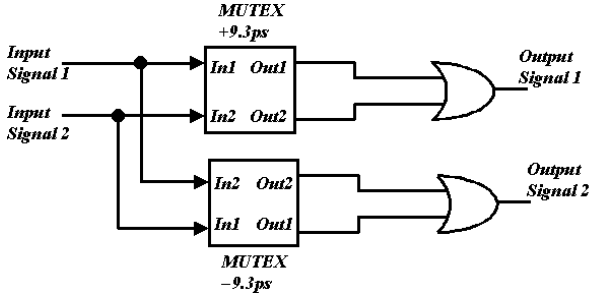

Fig. 7: MUTEX time offset for input range coverage

Fig. 8 shows the output characteristic of the Time Amplifier using the device dimensions shown in Table 1. In the graph a very linear response is obtained for the input range ± 6ps over the output range ± 60ps with consistent gain 10. This clearly indicates that the proposed Time Amplifier circuit is reliable as an amplifying element within the given range.

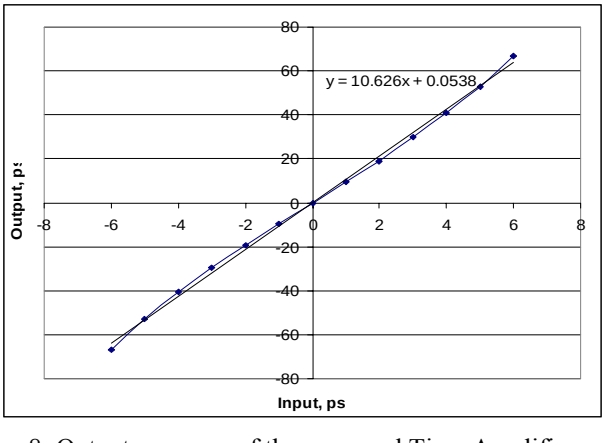

Fig. 8: Output response of the proposed Time Amplifier

6. Overview of the New TMC Scheme

Fig. 9 shows the block diagram of the new time measurement scheme. It has four main blocks which are: Time Amplifier, high-resolution TMC, coding circuit and calibration circuit. The high-resolution TMC and the Time Amplifier blocks use the same specifications as described in Section 5. The third block is the coding circuit. The function of this block is to capture the result of the TMC and convert the code based on the needs of the interface circuitry. The fourth block, essential for the correct measurement process, is the calibration circuit. The block consists of several sub-circuits which will be described in the following section.

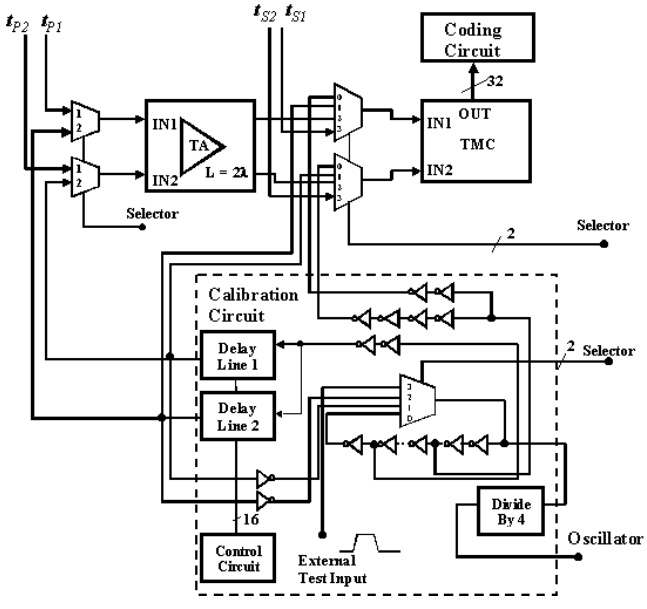

Fig.9: Proposed block diagram of the new TMC

a. Calibration Block

The function of the calibration block is to determine three circuit specifications, which are: the resolution of the TMC, the gain of the Time Amplifier and the input linear range of the Time Amplifier. The precise values obtained for the specifications will also give the precise result of the time measurement process. Therefore several supporting circuits and external test equipment, such as a high frequency counter are required. The supporting circuits needed in the calibration process are: a two-inverter delay, a ring oscillator, two divide by 4 circuits, a picosecond timing generator and a control circuit as shown in Fig. 9.

The first circuit involved in the calibration process is a ring oscillator. This is a simple technique [1] that has been used to measure the time constant of one inverter gate. The odd number of inverter gates in the ring loop causes the circuit to oscillate with a frequency of:

$$f_1 = \frac{1}{2.n.\tau_p} \qquad (7)$$

where f_1 is the output frequency, n is the total number of inverter gates and τ_p is the time constant of the inverter

gate. The estimated frequency for the ring oscillator using a 0.18 μm CMOS process is in the range of 30 to 50 MHz. To ease the measurement of the frequency of the oscillator using an external high-speed frequency counter, the oscillator frequency is divided down using a divide-by-4 circuit, thus:

$$F = \frac{f_1}{4} = \frac{1}{8.n.\tau_p} \qquad (8)$$

where F is the frequency measured at the output of the divide-by-4 circuit.

The next circuit is called a two-inverter delay. This circuit is a simple technique to generate two test signals with a known timing interval. When a rising signal is applied at the input of the two- inverter delay, two rising signals, signal 1 and signal 2, are generated at the outputs. The timing of the two signals is such that: signal 1 is faster than signal 2 by two inverter delays. If the same size of inverter circuit is used as in the ring oscillator circuit, the timing interval between the signals is approximately equivalent to $2.\tau_p$.

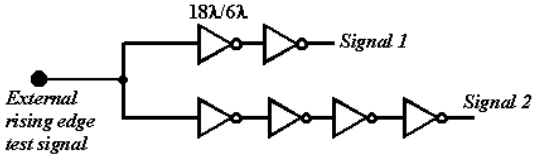

Fig. 10: Two-inverter delay

The third circuit involved in the calibration process is a picosecond timing generator. Two controllable high-resolution delay lines are used, each set with a different delay. When a single test signal is propagated through the two delay lines, the outputs from the two delay lines produces two test signals timed accurately to within a few picoseconds. Moreover, if the resolution of the two controllable delay lines is sufficiently small, a series of test signals with time intervals of a few picoseconds can easily be generated. Two high resolution programmable delay lines, using an Inverter Matrix or NMOS delay line, as reported in [5] and [2] respectively, are high-resolution timing delay lines which can perform the operation of the timing test generator. In order to measure the delay setting of the two delay lines, each delay line needs to be switched into the loop of the ring oscillator. The frequency output of the ring oscillator is measured to calculate the setting of the delay lines. The following equations formulate the calculations of the delay setting using the frequency outputs of the ring oscillator circuit for the two delay lines:

Delay line 1 $$F_1 = \frac{1}{4t_1} \qquad (9)$$

Delay line 2 $$F_2 = \frac{1}{4(t_1 + \Delta t)} \qquad (10)$$

Therefore $$\Delta t = \frac{(F_1 - F_2)}{4(F_1 F_2)} \qquad (11)$$

Where F_1 is the frequency of delay line 1, F_2 is the frequency of delay line 2 (both measured at the output of the divide-by-4 circuit), t_1 is the time delay of delay line 1 and Δt is the time delay difference between delay line 2 and delay line 1. In the oscillator circuit, when the delay line is calibrated, two delay parameters are varied, these are the rising edge (t_{LH}) and the falling edge (t_{HL}). However, in the test signal generator circuits, the rising edge is only involved in the delay difference between test signal 1 and test signal 2.

Assuming that t_{HL} and t_{LH} are equal. Therefore, when an external rising edge signal is activated at the external pin this would result in two rising signals with the timing delay (T_D) as:

$$T_D = \frac{t_{LH} + t_{HL}}{2} = \frac{\Delta t}{2} \qquad (12)$$

Substituting Equation 11 in Equation 12 yields

$$T_D = \frac{(F_1 - F_2)}{8(F_1 F_2)} \qquad (13)$$

b. Coding Circuit

The thermometer code to binary converter (TCBC) converts the thermometer code generated by the TMC to its binary equivalent. Converting the code immediately after the completion of the measurement process significantly reduces the size of the coding block.

7. Calibration Simulation Results

The first step in the calibration process is to activate the ring oscillator. The ring oscillator consists of 163 inverter gates and a divide-by-4 circuit oscillating with a period of 64.688ns. Using Equation 8 the propagation time of an inverter gate delay can be calculated as:

$$\tau_P = \frac{64.688ns}{4 * 2 * 163} = 49.6\text{ps}.$$

The next step is to estimate the resolution of the TMC. A rising edge is applied at the external pin to activate the outputs of the two-inverter delay circuit. From the first step it can be estimated that the time interval of the two-inverter delay circuit should be $2.\tau_p$ = 99.2ps. The 32-bit TMC generates the result 11111111111111111111000000000, which is equal to 21 in decimal. Based on the two values, the resolution of the TMC for each cell is approximately equal to $99.2ps/21 \cong 5ps$. The third step is to determine the gain of Time Amplifier. In the simulation process two Time Amplifier circuits were employed with different gain settings. Five test signals are applied and each test signal requires four values to be recorded, namely the loop frequencies of the delay lines 1 and 2 (F_1 and F_2), and the TMC outputs for Time Amplifiers 1 and 2 (T.A. 1, T.A. 2). F_1 and F_2 are used to estimate the approximate timing delay of the two test signals generated from the two delay line circuits. The results of the measurements and the calculations are tabulated in Table 2. This table is used to plot the graph of Fig. 11. From the graph it can be estimated that the gain of Time Amplifier 1 is ≅10.8 and of Time Amplifier 2 is ≅13.3. To justify the accuracy of the graph, the output waveforms of the two Time Amplifier circuits were

probed as shown in Fig. 12. The gain for Time Amplifier 1 is $36/3.5 = 10.3$ while for Time Amplifier 2 the gain is $53/3.5 = 15.1$. The accuracy of the first graph is 95.1 % while that of the second graph is 88.1 %. The graph also confirms that the linear range of the Time Amplifier is beyond the minimum range of the TMC at 5ps. This is enough to justify the requirement of the overlapped input range of the two circuits as illustrated in Fig. 6.

T_D (ps)	TA 1 (ps)	TA 2 (ps)
0	0	0
3	28.2	42.3
3.5	32.9	51.7
4	37.6	61.1
4.5	45	70.5
5	51.7	65.8
5.5	56.4	70.5
6.5	70.8	88.5

Table 2: Calibration simulation result

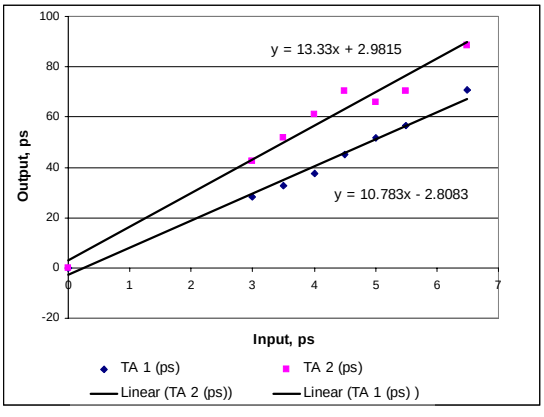

Fig. 11: Linearity gain of Time Amplifier circuits

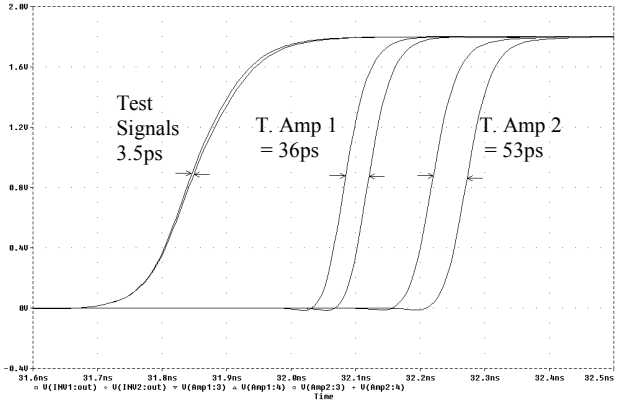

Fig. 12: Two Time Amplifier outputs

As a consequence the first Time Amplifier was chosen to combine with high-resolution TMC due to its high accuracy and gain (≅10). Thus the combination of the two circuits gives a ratio between the gain and the resolution of TMC as 2:1 (gain 10 against 5ps resolution of TMC). This ratio makes the minimum scale and resolution that can be measured by using the new scheme for time measurement as 0.5ps.

8. Final Layout Structure of Test Chip

The final layout, shown in Fig. 13, has the following specification: Number of Pads: 26, Chip area: 0.2 mm^2

9. Conclusion

A new TMC has been developed and described. The TMC comprises two novel circuit blocks: a Time Amplifier circuit and a high-resolution TMC. The Time Amplifier is capable of stretching small timing signals, which are then measured accurately by the high-resolution TMC. The results from the simulation analysis show that the new TMC is capable of measuring timing intervals as small as 0.5ps. The chip layout of the TMC has also been designed. The TMC is fast, occupying a small area of 0.2 mm^2 and completely digital, this makes the design very attractive for BIST applications for testing high-speed devices. Moreover the design also has an expandable input range, one shot measurement, and a synthesizable circuit design.

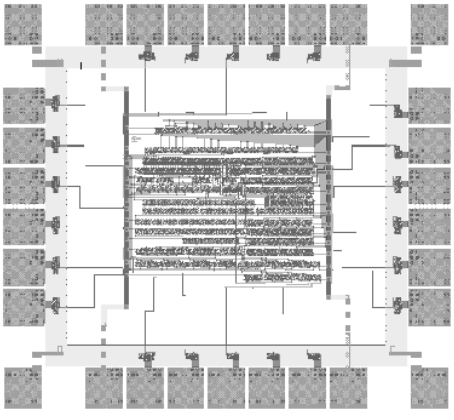

Fig. 13: Microphotograph of new TMC

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