# Synthesis for Manufacturability: a Sanity Check *

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## Abstract

*As we move towards nanometer technology, manufacturing problems become overwhelmingly difficult to solve. Presently, optimization for manufacturability is performed at a post-synthesis stage and has been shown capable of reducing manufacturing cost up to 10%. As in other cases, raising the abstraction layer where optimization is applied is expected to yield substantial gains. This paper focuses on a new approach to design for manufacturability: logic synthesis for manufacturability. This methodology consists of replacing the traditional area-driven technology mapping with a new manufacturability-driven one. We leverage existing logic synthesis tools to test our method. The results obtained by using STMicroelectronics $0.13\mu m$ library confirm that this approach is a promising solution for designing circuits with lower manufacturing cost, while retaining performance. Finally, we show that our synthesis for manufacturability can achieve even larger cost reduction when yield–optimized cells are added to the library, thus enabling a wider area-yield tradeoff exploration.*

## 1. Introduction

Traditionally, design methodologies (and the supporting tools and flows) for Integrated Circuits target nominal designs. However, defects and variations present in the IC manufacturing process may cause the circuit to behave differently from the nominal design in a substantial way. In particular, in deep submicron technologies, manufacturing process variations and defects may turn a successful design into a failure. Design For Manufacturability (DFM) is of strategic importance to decrease VLSI IC's manufacturing cost. DFM methods allow to estimate yield and robustness during the design phase, prior to manufacturing.

Yield is defined as the percentage of manufactured products that meet all performance and functionality specifications. Parametric yield loss usually refers to the effects on circuit performance caused by process variations; functional (or catastrophic) yield loss refers to physical and structural defects that cause the circuit to fail completely.

In deep-submicron new technology nodes, yield improvement is as much a design problem as it is a manufacturing problem. Presently, manufacturing optimization is performed at a post-synthesis stage: first synthesis targets area and timing [2, 1], then the design is optimized for yield at the layout level. This optimization might involve adding redundancy to contacts and vias, modifying the spacing between existing interconnections, and replacing cell instances with higher yielding variants, placed in the same position as their original ones. The reason placement is not perturbed is to avoid costly repetition of the optimization aimed at maximizing speed and minimizing area. Traditional post-synthesis yield optimization has been shown capable of reducing manufacturing cost by up to 10% [5, 10].

Extensive work has been devoted to understanding circuit sensitivity to these failure mechanisms and to reducing catastrophic yield loss [7, 6, 3, 4, 8, 9]. Heineken et al. [5] present an attempt to make this optimization less of an artwork process. In their approach, yield-optimized cells are generated and then substituted in the synthesized design. However, their algorithm is limited to an in-place substitution to preserve the footprint of the original design.

Following the general rule that the higher the level of abstraction the larger the horizon for optimization, we propose a *synthesis for manufacturability* approach, in which manufacturability is part of the cost function that drives synthesis. The necessity of including manufacturability (and testability) in the synthesis cost function was advocated in Shaik et al. [11], but, to the best of our knowledge, we are the first to address this issue.

The paper, focused on a synthesis-based methodology to improve functional yield loss, is organized as follows: Section 2 briefly introduces the new approach we propose, Section 3 provides some background on the catastrophic yield modeling problem, Section 4 reports the heuristics we implemented and the related experimental results are described in Section 5.

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## 2. Synthesis For Manufacturability

The current "yield-aware" design flow (Figure 1.a) [2, 1] is an optimization process with two main objectives: maximum speed and minimum area. The design is then processed for yield enhancement at the layout level. The new design paradigm we propose is illustrated in Figure 1.b: manufacturability is introduced to replace area in the cost function. The advantages of this approach are presented in Section 5.1. Clearly this new approach is transparent to designers who will only have to choose whether to target minimum area or minimum manufacturing cost.

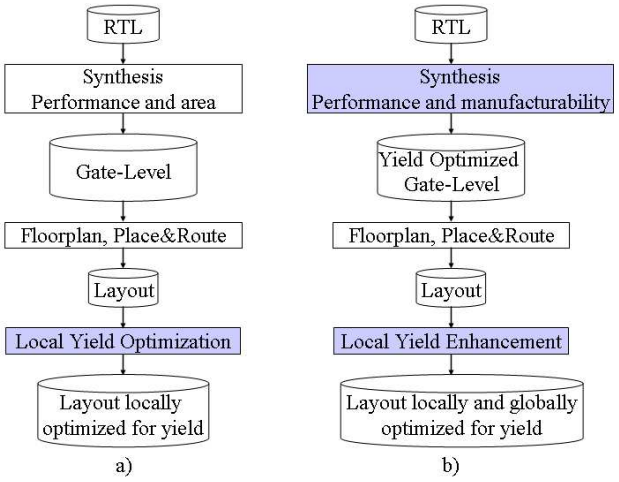



**Figure 1. a) Standard flow and b) Synthesis for manufacturability approach**

A further development to the new design for manufacturability paradigm is to incorporate yield during standard cell design: in addition to variants for high speed and low power, variants for high yield could also be included. In Section 5.2, we report a preliminary analysis on how our new technology mapping heuristics could exploit these libraries with yield-optimized variants to reduce manufacturing cost.

Comparing Figures 1.a and 1.b, one can observe that our approach focuses on choosing the best gate mapping prior to physical synthesis as opposed to manually or semi-automatically perform an in-place optimization limited by the design placement. This methodology is a global optimization and can be effectively complemented by traditional local optimization once the design has been layed out. Clearly, additional improvements can be achieved during the routing phase (e.g. [6]). Other circuit techniques, such as adding redundancy to render the circuit robust to failure [8], are also out of the scope of this paper.

In our approach, performance is still the first target during optimization. In fact, as the standard flow tries to optimize area on non-critical paths, the synthesis for manufacturability approach tries to optimize manufacturability (a combination of area and layout sensitivity to defects) on non-critical paths as well.

## 3. Background

In this Section we briefly review the catastrophic yield modeling problem definition: the focus is not on a rigorous statistical modeling for yield prediction, rather we intend to provide an intuitive view that will lead us to understand the new cost function we use propose to use during synthesis and the related results.

Various different types of *defects* are introduced during the manufacturing process. These defects may, for example, result into open or short circuits. However, not all defects will necessarily cause a circuit failure: functional yield loss depends, in fact, on the wafer defectivity and on the design attributes.

The figure that is commonly used to quantify layout sensitivity to defects is the critical area. Critical area $A_i^c(x)$ for defects of type $i$ and diameter $x$ is defined as the size of the area in which the center of defect of type $i$ and diameter $x$ must fall in order to cause a circuit failure. We indicate as $A_i^c$ the critical area for defects of type $i$ averaged over all defect diameters $x$:

$$A_i^c = \int A_i^c(x) f_d(x) dx \tag{1}$$

where $f_d(x)$ is the defect probability density function.

Finally, let $d_i$ denote the average number of defects of type $i$ per unit area, then the average number of faults on the circuit is:

$$\lambda = \sum_i A_i^c \cdot d_i \tag{2}$$

where the sum is taken over all possible defects types on the circuit [8].

It can be shown that, in general, for a given design component $b$, yield may be expressed as:

$$Y_b = e^{-\lambda_b} \tag{3}$$

where $\lambda_b$ is the *failure rate* of component $b$.

Assuming that gates are statistically independent components and defects are uniformely distributed (Poisson model), yield for a circuit with $N$ gates, can be expressed as:

$$Y_{circuit} = \prod_{k=1}^{N} Y_{G,k} \tag{4}$$

where $N$ is the number of circuit gates and $Y_{G,k}$ is the yield of a single gate averaged with respect to different defect

types and size. Referring to Equation (3), the circuit yield becomes:

$$Y_{circuit} = e^{-\sum_{k=1}^{N} \lambda_{G,k}} = e^{-\lambda_{circuit}} \quad (5)$$

It has been shown that this model is pessimistic for yield values *prediction* due to the fact that defects are not uniformely distributed, but rather tend to cluster.

There is a vast literature (e.g. [8, 12]) on how to derive a model to accurately predict yield with clustered defect distributions. Nevertheless, our research is aimed at analyzing how synthesis for manufacturability can *lower manufacturing cost* rather than doing an exact yield prediction. Therefore, we will use the simple Poisson model (4) together with the failure rate description (5) to focus on yield increase/decrease rather than its exact value.

Finally, it is important to make a distinction between the *effective yield* of a circuit $Y_{eff,circuit}$, defined as the number of "good" circuits per wafer and the yield of a circuit $Y_{circuit}$ defining the percentage of "good" circuits. They are related through the equation:

$$Y_{eff,circuit} = N_{circuit} \cdot Y_{circuit} \quad (6)$$

where $N_{circuit}$ is the number of circuits in the wafer.

To lower the manufacturing cost of a circuit we need to improve its effective yield, that is to achieve a better trade-off between yield and the actual number of circuits that can fit in a given wafer area.

Recalling Equations (2) and (3) we can observe that yield loss is due to the combination of two effects: the presence of a defect and the sensitivity of the component to the defect. Assuming we cannot influence the defect distribution, we are left to decrease the circuit sensitivity and perform a trade-off with circuit area: this is the goal of synthesis for manufacturability.

## 4. Technology Mapping Heuristics for Manufacturability

This Section presents different heuristics analyzed to implement our new synthesis for manufacturability approach depicted in Figure 1.b. The goal is to have an indication of the usefulness of this approach: this preliminary exploration phase is based on the modification of the well-estabilished technology mapping algorithm available in commercial tools such as Synopsys Design Compiler [1]. Given the fact that performance is the primary objective, some flexibility is left on area along the non-critical paths: the key idea is to exploit this flexibility to obtain a higher effective yield by manipulating yield and area instead of simply area.

In state-of-the-art tools, technology mapping is performed using a dynamic programming algorithm which relies on the fact that area is an additive funtion. Things are not so straightforward for effective yield. In fact, assuming wafer area $A_{wafer}$ is given, for synthesis for manufacturability the optimization problem becomes:

$$max \quad \frac{Y_{circuit}}{A_{circuit}} = \frac{\prod_{k=1}^{N} Y_{G,k}}{\sum_{k=1}^{N} A_{G,k}} \quad (7)$$

or equivalently:

$$min \quad \frac{A_{circuit}}{Y_{circuit}} = \frac{\sum_{k=1}^{N} A_{G,k}}{\prod_{k=1}^{N} Y_{G,k}} \quad (8)$$

where $A_{circuit}$ and $Y_{circuit}$ are area and yield of the circuit respectively, while $A_{G,k}$ and $Y_{G,k}$ are area and yield of the single gates composing the circuit. The cost function for the optimization problem described in Equation (8) is not simply additive and therefore we need to devise a good heuristic to approximate it.

Here we report some observations on different heuristics and in Section 5, we provide the corresponding experimental results.

**Heuristic 1: Yield Only.** An intuitive approach would be to try to improve circuit yield by decreasing layout sensitivity to defects as described by Equations (2) and (3). Therefore, recalling Equations (5) and (4), the optimization problem becomes:

$$max \quad \prod_{k=1}^{N} Y_{G,k} = e^{-\sum_{k=1}^{N} \lambda_{G,k}} \quad (9)$$

or its equivalent additive form:

$$min \quad |ln(Y)| = |ln(\prod_{k=1}^{N} Y_{G,k})| = \sum_{k=1}^{N} \lambda_{G,k} \quad (10)$$

In practice, this would mean to minimize the critical area (or equivalently the failure rate), disregarding the actual circuit area.

**Heuristic 2: Weighted Yield.** While in the previous heuristic area is not taken into account, it can be easily introduced as a weigthing factor in equation (10) and turn the optimization problem into:

$$min \quad \sum_{k=1}^{N} |A_{G,k} ln(Y_{G,k})| = \sum_{k=1}^{N} A_{G,k} \lambda_{G,k} \quad (11)$$

**Heuristic 3: Manufacturability Function Approximation.** A more sophisticated approach is to approximate the original cost function as closely as possible with an additive function. We adopt the following approximation for the optimization problem:

$$min \ \frac{A_{circuit}}{Y_{circuit}} = \frac{\sum_{k=1}^{N} A_{G,k}}{\prod_{k=1}^{N} Y_{G,k}} \approx min \ \sum_{k=1}^{N} \frac{A_{G,k}}{Y_{G,k}^{p}} \quad (12)$$

where $p$ is a parameter that can be chosen to tune up the heuristic.

An intuitive choice is $p = 1$, but we will show that $p = N$ is actually a better value. The reason for choosing $p = N$ becomes evident if we approximate all $Y'_{G,k}s$ with a common average value $Y_a$ [1]:

$$\sum_{k=1}^{N} \frac{A_{G,k}}{Y_{G,k}^N} \approx \frac{\sum_{k=1}^{N} A_{G,k}}{Y_a^N} = \frac{\sum_{k=1}^{N} A_{G,k}}{\prod_{k=1}^{N} Y_a} \approx \frac{\sum_{k=1}^{N} A_{G,k}}{\prod_{k=1}^{N} Y_{G,k}}$$

We explored different values of $p$ and experimental results are reported in Section 5.

## 5. Experimental Results

As we mentioned in Section 2, the synthesis for manufacturability can be envisioned in two steps: the first is to change the synthesis cost function to include yield and the second is to enrich the standard cell library with yield-optimized gates.

In Subsection 5.1 we show that significant improvement can already be achieved at no-cost for designer and library developers, i.e. by only changing the synthesis cost function. Further reduction of manufactuting cost can be obtained when yield-optimized gates are added to the library (similarly to having speed-optimized or low-power versions): preliminary results are reported in Subsection 5.2.

### 5.1. Technology mapping for manufacturability

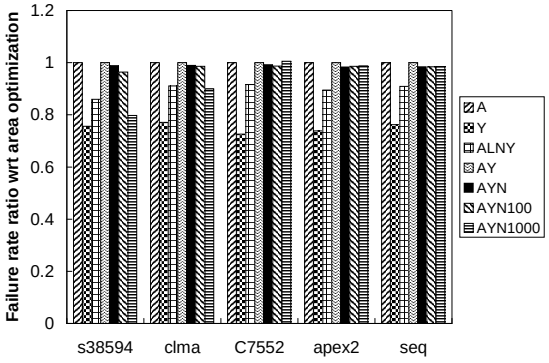
We evaluated the different heuristics proposed in Section 4 on testcases from the IWLS93 benchmark suite mapped on STMicroelectronics $0.13\mu m$ standard cell library. Since yield data for the standard cell library were not available to us, we assigned a yield value to each gate by assuming the failure rate $FR$ to be a random variable with a uniform distribution in $(300ppb, 500ppb)$.

Results from heuristics evaluation are reported in Figure 2: the bottom table explains the correspondence between the symbols in the legend and the function used as heuristic.

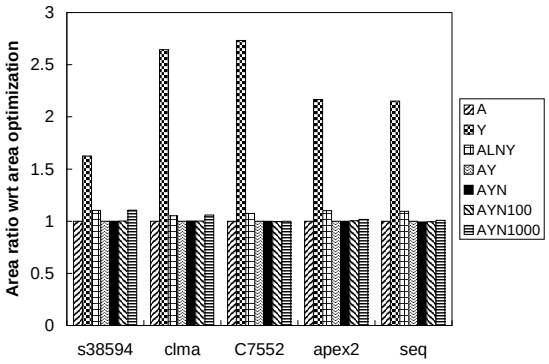
Figure 2 reports the failure rate (a), the area (b) and the effective yield (c) normalized to values obtained from the standard synthesis optimization based solely on area (indicated as $A$).

These data confirm the observations we reported in Section 4: the best results for failure rate reduction are obtained by performing optimization solely based on yield ($Y$) and secondly by using yield weighted by area ($ALNY$). Nevertheless, as expected, these heuristics perform poorly for area: overall, the effective yield is worsened by these

1 This approximation seems reasonable given the typical values of $Y_{G,k} = e^{-FR_{G,k}} \simeq 1 - FR_{G,k}$ with $FR_{G,k} << 1$.




a)

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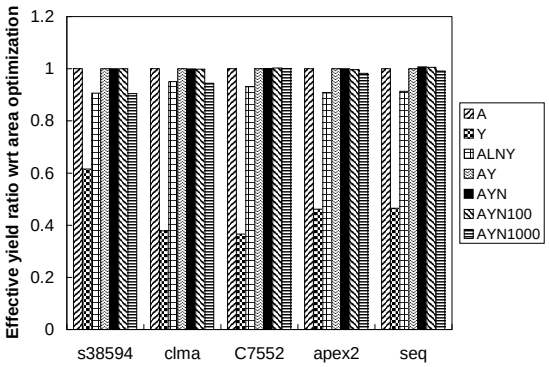



c)

| Symbol | A | Y | ALNY | AY |
|---|---|---|---|---|
| Heuristic | $A$ | $\|ln(Y)\|$ | $\|A \cdot ln(Y)\|$ | $A/Y$ |

| Symbol | AYN | AYN100 | AYN1000 |
|---|---|---|---|
| Heuristic | $A/Y^N$ | $A/Y^{100N}$ | $A/Y^{1000N}$ |

**Figure 2. Comparison of different heuristics for synthesis for manufacturability on IWLS93 benchmark. Data are normalized with respect to results obtained with the standard synthesis flow.**

| Function | *s38584* | *clma* | *C7552* | *apex2* | *seq* |
|---|---|---|---|---|---|
| $A$ | 1 | 1 | 1 | 1 | 1 |
| $\|ln(Y)\|$ | 0.61 | 0.37 | 0.36 | 0.46 | 0.46 |
| $\|Aln(Y)\|$ | 0.90 | 0.95 | 0.93 | 0.90 | 0.91 |
| $A/Y$ | 1 | 1 | 1 | 1 | 1 |
| $A/Y^N$ | 1.0001 | 0.99 | 1.001 | 1.0002 | 1.006 |
| $A/Y^{100N}$ | 0.99 | 0.99 | 1.002 | 0.99 | 1.005 |
| $A/Y^{1000N}$ | 0.90 | 0.94 | 1.0009 | 0.98 | 0.99 |

**Table 1. Effective yield ratio with respect to standard synthesis optimization on IWLS93 circuits.**

heuristics (Figure 2.c and Table 1). The last four colums of the chart correspond to different values of $p$ using the heuristic in Equation (12). Table 1 confirms the results predicted in the previous Section: assuming yield follows a Poisson model, $p = N$ leads to best results for effective yield. As an additional remark, the error due to the approximation described in Equation (12) is less than $0.1\%$ with $p = N$, while it can reach values up to $20\%$ by using $p = 100N$. Furthermore, results from a number of other testcases from the IWLS93 benchmark, confirm the validity of choice $p = N$: therefore, we will use this heuristic to drive our technology mapping algorithm in the following experiments. Notice that, $AY$ gives the same results as the standard optimization for area. This is due to the fact that for a single gate, yield $Y = e^{-FR}$ is "almost" 1. These high yield values for the single cell are the reason why we explored giving larger importance to yield, by using $p = 100N$ and $p = 1000N$.

It is worth noticing that the circuits reported above are quite small and this explains the relatively small improvement in effective yield. To evaluate the impact that synthesis for manufacturability can have on larger circuits, we created a $1cm^2$ circuit constituted of a repetition of a single circuit (called seed).

We estimated the projected effective yield value on $1cm^2$ circuits by using as seed for replication some IWLS93 circuits. Results are reported in Figure 3: effective yield improvement can be as large as $9\%$. As a final observation, it is worth recalling that this substantial improvement is obtained at absolutely no cost for designers and library developers, assuming yield information are available.

### 5.2. Further improvement: yield-optimized gates

As we already mentioned, results obtained in Section 5.1 can be further improved by using libraries with yield-optimized variants in addition to the cells optimized for speed and/or area.

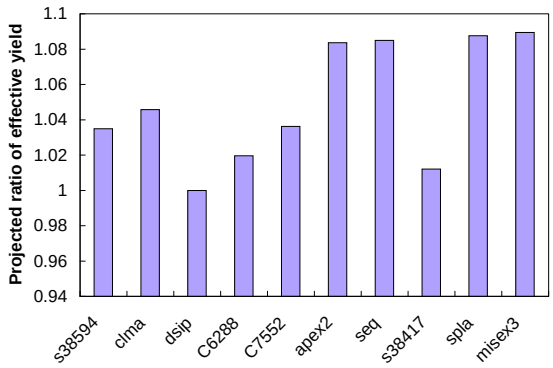



**Figure 3. Projection of results of synthesis for manufacturability on repetition of seed circuits to constitute a $1cm^2$ area.**

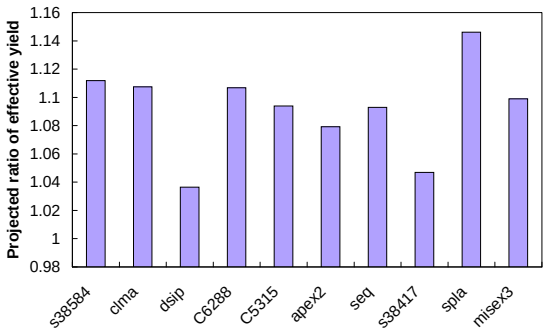
To show how this can lead to a higher effective yield, we developed a virtual variant for each of the original standard cells from the STMicroelectronics $0.13\mu m$ library. Yield improvement has been modeled by using a random variable $FR\_factor$ with a uniform distribution in $(1, 10)$ to divide the original cell failure rate $FR$. In other words, for each cell, the new variant's failure rate will be decreased randomly from a value in $(300ppb, 500ppb)$ to a value in $(30ppb, 500ppb)$. According to past literature [5], manufacturability can be improved with small or no penalty in area (or even area reduction). We assumed that $80\%$ of cell variants will suffer from area increase, while the remaining $20\%$ will benefit from yield increase with no area penalty. Clearly this is a conservative assumption and better results can be achieved with more advantageous trade-offs. The cells to suffer from area penalty are chosen randomly and area is increased by a discrete quantity (technology pitch multiplied by the cell height).

Circuits from the IWLS93 benchmark were synthesized on the enhanced library containing both the original cells and the high-yield variants. Both the standard flow (optimization for area) and synthesis for manufacturability have been used (implementing heuristic $AYN$).

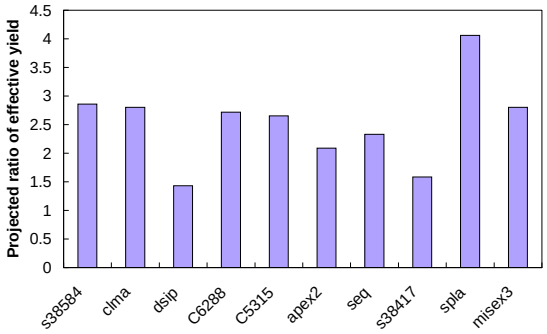
As done in the previous Subsection, to obtain a projection of effective yield improvement on large circuits we replicated the IWLS93 circuits to form $10mm^2$ (Figure 4.a) and $1cm^2$ (Figure 4.b) areas. Data show that a substantial effective yield improvement can be obtained by using the synthesis for manufacturability flow on the extended libraries.

**Remarks** All the experiments are based on the Poisson yield model. As discussed in Section 3, this model typically produces a lower bound on the effective yield.

The goal of this paper is to highlight the trend of manufacturability improvement that can be obtained using the




a)




b)

**Figure 4. Projection of the ratio of effective yield using IWLS93 benchmark to obtain $10mm^2$ a) and $1cm^2$ b) circuits. Data are normalized with respect to results obtained by using the standard synthesis flow.**

new heuristics for the technology mapping algorithm. Although we do not compute exact yield values, we expect that an increase in yield lower bounds will also lead to a decrease in the defect sensitivity and to an increase of yield exact values. Hence, a more accurate yield model is expected to give a similar trend.

Finally, when using different yield and process models, we can either use a different heuristic to better match data, or we can simply tune the value of $p$ in Equation (12). In fact, we have shown that increasing $p$ increased the weight of yield in the manufacturability cost function.

## 6. Conclusions

Methodologies to increase manufacturability are of utmost importance to lower manufacturing costs for deep submicron technologies. Post-layout optimization has a limited impact, hence we propose a new synthesis for manufacturability approach to target effective yield early in the design stage. Different heuristics for technology mapping have been presented to implement this methodology using Synopsys Design Compiler. The new approach is completely transparent to designers and library developers and results on the IWLS93 benchmark show it may lead to significant effective yield improvement. Further cost reduction is observed by extending the standard cell library to include yield-optimized variants and using the new technology mapping heuristics.

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