Crosstalk Minimization in Logic Synthesis for PLA

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Abstract

We propose a maximum crosstalk minimization algorithm taking logic synthesis into consideration for PLA structure. To minimize the crosstalk, technique of permuting wire is used which includes the following steps. First, product lines are partitioned into long set and short set, and then product lines in long set and short set are interleaved. By interleaving algorithm, an upper bound on the maximum coupling capacitance of the product lines can be derived. Then, we take advantage of crosstalk immunity of product lines in long set to further reduce the maximum crosstalk effect of the PLA. Finally, synthesis techniques such as local transformation and global transformation are taken into consideration to search for a better result. The experiments demonstrate that our algorithm can effectively minimize the maximum crosstalk effect of a circuit by 48% as compared with the original area-minimized PLA without crosstalk minimization.

I. Introduction

In deep submicron (DSM) technology, coupling capacitance grows exponentially to the down-sizing of the feature size. The crosstalk effect as such will result in unpredictable timing and at worst give incorrect result. Therefore, the minimization of crosstalk is becoming an important issue today [1] [2] [3] [4]. In general, the most effective technique is to minimize crosstalk by permuting wires so that the coupling length among all wires are minimized.

Dynamic Programmable Logic Array (Dynamic PLA) as a well developed structure [5] [6] [7] [8] [9] is divided into two planes, AND-plane and OR-plane. In AND-plane, inputs are computed to form product terms while in OR-plane, product terms are summed up to generate outputs. Due to the regularity of a PLA, it is much easier to estimate the area and delay as compared to cell-based and full-custom design methodology. This characteristic makes PLA an attractive alternative to implement logic in DSM era. For example, taking advantage of its predictable delay, Khatri and Brayton proposed an unique design methodology for DSM technology by utilizing PLA structure [5].

Unfortunately, the coupling capacitance between long parallel wires in PLA may cause serious crosstalk effect. That makes synthesizing a PLA taking crosstalk effect into consideration an important issue. There are several researches addressing this topic [3] [5] [10]. In [5] [10], dense wiring fabric (DWF) was designed to reduce crosstalk by power/ground line insertion for PLA. In [3], Tien and Chang proposed a PLA product-term ordering algorithm to maximize crosstalk immune (CT-immune), i.e., that the crosstalk effect between adjacent CT-immune product terms can be ignored if they activate the same outputs. [3] has the drawback that it strongly relies on the dominance relationship of product lines in the OR-plane to build a CT-immune graph.

For crosstalk minimization, most of previous researches focus on minimizing the total wire coupling capacitance [1] [2] [3]. However, the wire with the maximum crosstalk effect is the most likely victim of a circuit. The total crosstalk does not reflect this effect. Therefore, to prevent a circuit from malfunctioning due to crosstalk effect, we will consider minimizing the maximum coupling capacitance of a circuit instead. To that end, technique of permuting product line is used which includes the following steps. First, product lines are partitioned into long set and short set, and then product lines in long set and short set are interleaved. By interleaving algorithm, an upper bound on the maximum coupling capacitance of the product lines can be derived. Then, we take advantage of crosstalk immunity of product lines in long set to further reduce the maximum crosstalk effect of the PLA. Finally, synthesis techniques such as local transformation and global transformation are taken into consideration to search for a better result.

The rest of the paper is organized as follows. Some preliminary background and motivation of this work are given in Section 2. Section 3 presents long set and short set operations for minimizing the maximum coupling capacitance. Two logic level transformations to find a better result is proposed in Section 4. Our experimental results are shown in Section 5. Section 6 concludes this work.

II. Motivation

A. PLA Crosstalk Formulation

The crosstalk effect between two parallel wires is derived as follows [11]:

$$crosstalk\_effect \propto coupling\_capacitance \propto \frac{coupling\_length}{wire\_distance^2} \quad (1)$$

where *coupling_length* and *wire_distance* are the overlapping length and vertical distance, respectively, between two wires.

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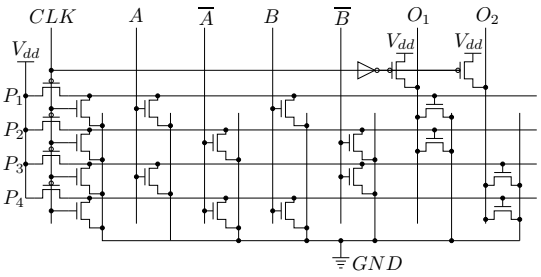

Fig. 1. Dynamic PLA schematic view.

From Equation (1), it is observed that the coupling capacitance decreases quadratically to the wire distance of two wires. Therefore, we will consider only the crosstalk effect of two neighboring wires.

A schematic view of a dynamic PLA core in [8] is shown in Figure 1. To compute the crosstalk effect of the PLA, wires of I/O columns and the product-term rows need to be considered. However, because I/O columns are interleaved with ground wires and the ground wires provide good shielding for crosstalk prevention, the crosstalk effect among I/O columns can be ignored. For the product-term wires, due to the monotonic phase transition characteristic of dynamic PLA, crosstalk effect should be taken seriously. For example, during precharge stage, output wires are charged to high while product terms are discharged to low [8] [9]. Then, during evaluation stage, if an aggressor product term evaluates from low to high and discharges the output wire, a victim product-term wire may be accidentally charged to high due to crosstalk. It likely causes incorrect result due to discharge of the output wire.

In this work, we will focus on minimization of the maximum crosstalk effect between neighboring product-term rows. The *coupling_length* of two neighboring wires is computed by the number of columns crossed by the two product-term wires. Figure 2 gives an example of computing the maximum coupling wire length. The coupling length between two adjacent product terms P_1 and P_2 is $(P_1, P_2) = 10$. Similarly, coupling lengths of $(P_2, P_3) = 9$, $(P_3, P_4) = 2$, $(P_4, P_5) = 2$, $(P_5, P_6) = 7$. It can be seen that, P_1 and P_2 result in the maximum crosstalk effect of the PLA.

B. Motivation Example

The crosstalk effect of a dynamic PLA will be different if we utilize the permutation of wires and synthesis of different covers of the function. An example that illustrates how the two techniques affect the crosstalk effect is shown below.

Given a 5-input 5-output Boolean network, logic optimization tool, *Espresso*, is used to obtain a minimal cover C_1:

$$C_1 = \begin{cases} O_1 &= P_1 + P_4 + P_6 \\ O_2 &= P_5 + P_6 \\ O_3 &= P_1 + P_3 \\ O_4 &= P_1 \\ O_5 &= P_2 + P_3 + P_5 \end{cases}$$

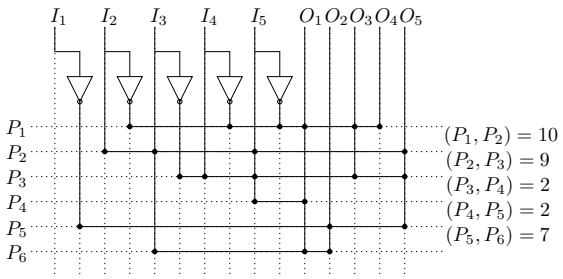

Fig. 2. Crosstalk effect of minimal cover C_1.

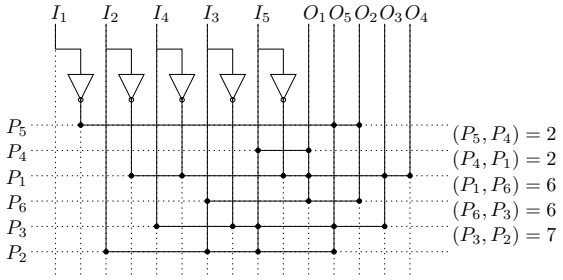

Fig. 3. Crosstalk effect of minimal cover C_1 after wire permutation.

where C_1 has 6 product terms, $P_1 = \overline{I_2 I_4 I_5}, P_2 = I_2 I_3 I_5, P_3 = \overline{I_3} I_4 I_5, P_4 = I_5, P_5 = \overline{I_1}$, and $P_6 = I_3$. If the PLA is synthesized without I/O and product-term permutation, the maximum crosstalk is 10 as shown in Figure 2. If the I/O and product wires are permuted, the resultant PLA is shown in Figure 3, where the maximum crosstalk becomes 7. Furthermore, if the function is re-synthesized to a different cover, C_2:

$$C_2 = \begin{cases} O_1 &= P_1 + P_4 + P_5 + P_6 \\ O_2 &= P_2 + P_3 + P_5 \\ O_3 &= P_1 + P_4 \\ O_4 &= P_4 \\ O_5 &= P_1 + P_2 + P_3 \end{cases}$$

where C_2 also has 6 product terms, $P_1 = \overline{I_3} I_4 I_5, P_2 = I_1 I_2 I_3 I_5, P_3 = \overline{I_1}, P_4 = \overline{I_2 I_4 I_5}, P_5 = I_3$, and $P_6 = \overline{I_3} I_5$ as shown in Figure 4. With this new cover, C_2, after I/O and product-term permutation are performed, the resultant PLA is shown in Figure 5. In this case, the number of product terms remains the same but the maximum crosstalk is reduced from 7 to 5.

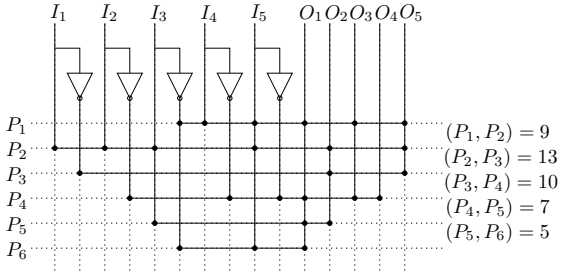

Fig. 4. New cover C_2.

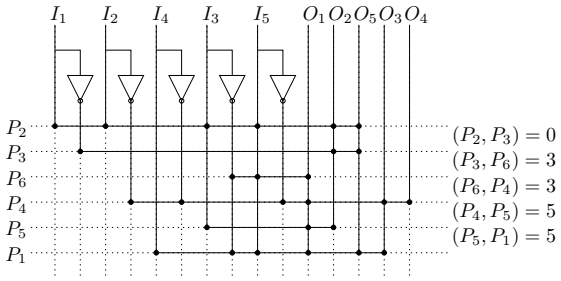

Fig. 5. Crosstalk effect of C_2 after wire permutation.

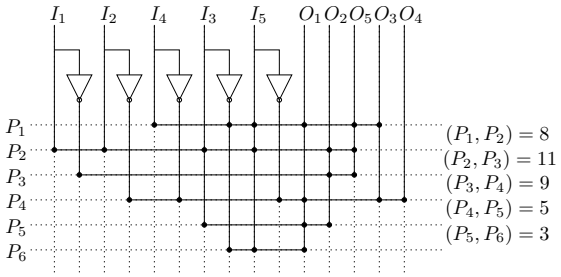

Fig. 6. Example of I/O ordering.

From the above-mentioned example, we know that a minimal cover does not guarantee to achieve the goal of dynamic PLA with minimum crosstalk effect. To reach that goal, not only an algorithm to permute I/O and product-term wires but also synthesis of different covers have to be considered.

III. PLA Crosstalk Minimization

The coupling length of two adjacent product terms is determined by not only the ordering of product terms but also the I/O ordering. A straight forward enumeration is to permute all I/O and product-term ordering. Obviously, that is not feasible for large size PLA. We propose a two-step algorithm to find a solution. In the first step, a good I/O ordering is searched. Then, in the second step, based on the I/O ordering found in the first step, product-term ordering is performed. The detailed algorithms for I/O and product-term ordering are discussed in the following.

A. I/O Ordering

I/O column is ordered by the number of product terms it engages. That is, the number of dots in each column. Columns with more dots are placed inward, otherwise they are placed outward [3]. The reason behind this heuristic is as follows. The number of dots gives the number of product terms the column engages. Moreover, the dots at two ends of a product term determine the wire length of that product. Ordering columns with less dots at two ends will reduce the number of product terms with long wire length. Figure 6 shows the PLA after I/O ordering out of that shown in Figure 4.

B. Long set and Short set Interleaving

Exhaustive search is infeasible to find a best product-term ordering because there are $N!$ possible ordering, where N is the number of product terms. We develop an efficient algorithm to order the product-term wires in order to minimize the maximum coupling capacitance of a PLA.

First, based on the I/O ordering obtained in the first step, we calculate the length of each product term. The length of a product term is the distance between the leftmost device in AND-plane and the rightmost device in OR-plane. Second, based on the length of the product terms, we partition them into two sets, long set, *long* and short set, *short*. The first $\lceil \frac{N}{2} \rceil$ longest product terms belong to *long*, and the remaining $\lfloor \frac{N}{2} \rfloor$ shortest product terms are assigned to *short*. Finally, we interleave the product terms in *long* and product terms in *short*. For example, assume *long* =$\{l_1, l_2, l_3, ...\}$ and *short* = $\{s_1, s_2, s_3, ...\}$. The product-term ordering will be l_1, s_1, l_2, s_2, l_3, s_3,..., and etc. By utilizing the interleaving ordering, the maximum coupling capacitance of PLA will be bounded by the longest product-term wire length in *short*. Moreover, the total crosstalk will be bounded by the total length of product terms in *short*.

The upper bound occurs when the product term in *short* is completed overlapping with the product term in *long*. For example, in Figure 3, P_6 is covered by P_3. The coupling length between P_6 and P_3 is determined by the length of P_6. However, when the product-term length in *short* is not covered by the length of the product term in *long*, the overlapping length is less than the length of the product term in *short*. For example, in Figure 3, P_2 is not covered by P_3. The coupling length is less than the wire length of P_2. Based the above observation, we can properly order the product terms in *short* and product terms in *long* to reduce the overlapping length. A heuristic is proposed as follows. First, the columns are numbered from left to right. For each product term, we compute the column position of its leftmost device in AND-plane. Then, product terms in *long* are sorted by the column position of the leftmost device in descending order while those in *short* are sorted in ascending order. Then, the product terms in *long* and *short* are interleaved. The heuristic tends to minimize the overlapping length between product terms in *long* and product terms in *short*.

Figure 7 shows the result out of the PLA shown in Figure 6 after performing ordering product line in *short* and in *long*, respectively, and then interleaving the product lines in *long* and in *short*.

C. Grouping in Long Set

Crosstalk immune between two wires was presented in [3]. The basic idea of crosstalk immune is as follows. Assume that there are two adjacent product terms activate the same outputs. One product term is an aggressor and the other is a victim. Let the aggressor evaluate from low to high while the victim remain low. Assume that crosstalk noise propagates to the victim and causes a transient high signal on victim line. The transient signal of the victim will be harmless to the

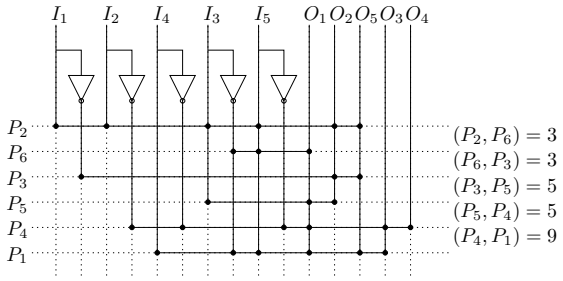

Fig. 7. Example of *long* and *short* interleaving.

Procedure *Grouping_in_Long_Set* (PLA)
Begin
partition PLA into *long* and *short*
for each product p not grouped in *long*
find $long' \subseteq long$, s.t. outputs in *long'* are same
create a *super-product-term* $p^{\dagger}$
$long = (long \cup p^{\dagger}) - long'$
$balance(long, short)$
end foreach
End

Fig. 8. The *Grouping in Long Set* procedure

output result because the output lines are to be discharged by the aggressor. Hence, the crosstalk effect between two adjacent product terms can be ignored if their output parts are the same.

We can utilize the crosstalk immune property to further reduce the crosstalk effect of a dynamic PLA. First, for a given product term in *long*, we group all other products in *long* that connect to the same output signals with this product to form a *super-product-term*. The product terms in a *super-product-term* will be viewed as a single product line. Then, we move the product terms in *short* to *long* such that the sizes of two sets are balanced. Note that we do not consider all the product terms for grouping as Tien and Chang [3] did. Instead, we only group those product terms in *long*. As a result, the grouping process can reduce the longest product-term length in *short*, that is, the maximum crosstalk effect of the PLA.

For example, given a PLA with N product terms. There are $\lceil \frac{N}{2} \rceil$ product terms in *long* and $\lfloor \frac{N}{2} \rfloor$ product terms in *short*. If m product terms can be grouped into a *super-product-term* in *long*, the number of product terms in *long* will become $\lceil \frac{N}{2} \rceil - m + 1$. Since the number of product terms in *long* is reduced, we balance the size of *long* and *short* by moving the first $\lfloor \frac{m}{2} \rfloor$ longest product terms from *short* to *long*. As a result, the longest length of product term in *short* as well as the maximum coupling length is reduced. The above grouping process would repeat until no product term in *long* can be grouped. This technique is very effective because we found that in many benchmarks, many product terms activate the same outputs.

Taking PLA shown in Figure 7 as an example, we demonstrate how to perform grouping in *long*. Initially, *long* = $\{P_2, P_3, P_4\}$ and *short* = $\{P_6, P_5, P_1\}$. Since P_2 and P_3 activate the same outputs, they are formed a *super-product-term*. To balance the size of two sets, the longest length product term in *short*, P_1, is moved to *long*. We can see that the longest length of products in *short* is reduced from 9 to 5. After interleaving the product terms in the new *long* and *short*, we have a PLA with the maximum crosstalk 5 as shown in Figure 5. The detailed procedure for grouping in long set is shown in Figure 8.

IV. Logic Synthesis for Crosstalk Reduction

Given a function, there are many different covers to represent the same function. Different covers will result in different maximum crosstalk effect after the same I/O ordering, product-term permutation and grouping algorithms are performed. To search a cover that minimizes the maximum coupling length, we propose two synthesis techniques, *local transformation* and *global transformation*, to search for a better cover. In *local transformation* and *global transformation*, the two-level logic optimization tool, *Espresso*, will be used as a core to find sum of product form of a given function.

A. Local Transformation

In *Espresso*, *REDUCE* step reduces the size of a product term while *EXPAND* step expands the size of a product term. For a reduced product term, expanding the product term to different directions will result in different primes [12]. In *local transformation*, iterative performing *REDUCE* and *EXPAND* on product term to select suitable product terms for crosstalk reduction is designed. In each iteration, a reduced product term is expanded to all possible primes. Then, the wire length for all alternatives are computed. To reduce crosstalk, the product term with shortest wire length is selected for expansion.

B. Global Transformation

Local transformation is applied to a given synthesis result. If the given initial synthesis result is not close to the global optimal, it is very difficult for *local transformation* to produce a good solution. Therefore, we propose a *global transformation* to synthesize different initial covers for *local transformation* to start with.

To produce different initial covers, *global transformation* begins with splitting the given PLA into several smaller PLAs. Then, each smaller PLA is optimized individually. Finally, the smaller PLAs are combined to form a single PLA.

To develop a method to split one PLA into several smaller ones, we split the multi-output PLA into several single-output PLAs and analyze the relationship between pairs of outputs. We found that it is preferable to group outputs with similar functionality. To measure the similarity of two functions, the number of common product terms of two functions are

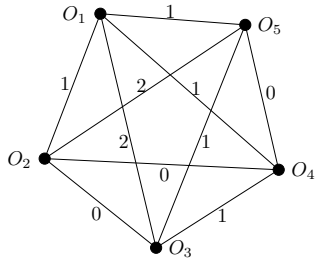

Fig. 9. Output Grouping Graph of Figure 4.

Procedure *Global_Transformation*(*PLA*)
Begin
group = output_grouping(OGG)
PLA_list = split(PLA, group)
optimize each *PLA* in *PLA_list*
PLA = combine(PLA_list)
optimize *PLA*
End

Fig. 10. The *Global Transformation* procedure

used. Therefore, the similarity of two outputs, $sim(O_i, O_j)$, is defined as:

$sim(O_i, O_j) =$ the number of common products in O_i and O_j.

After computing the similarity for all pairs of outputs, we model the relations of all outputs as a weighted complete graph *output-grouping-graph*, $OGG(V, E)$, where V represents output set and the weight on an edge (O_i, O_j) is defined as $sim(O_i, O_j)$. Figure 9 shows the *OGG* of the sum of product representation shown in Figure 4.

After *OGG* is built, we call *global transformation* iteratively. In each iteration, the two vertices with the maximum edge weight are selected and the two corresponding smaller PLAs are merged. After merging, we optimize each PLA individually, then combine all PLAs into a new PLA as a new initial cover. The above algorithm repeats until the *OGG* becomes a single-vertex graph. Figure 10 shows the procedure of *global transformation*. The overall *Find Minimum Crosstalk* algorithm is shown in Figure 11.

V. Experimental Results

Our experiment is performed on SUN-Blade1000 with 2 gigabytes of memory. Software platform is based upon the *Espresso* package in SIS [13]. MCNC benchmark suite is used in our experiments. The experiment is conducted to find the minimum crosstalk effect of a circuit. First, *Espresso* is used to generate a PLA cover with minimal area cost. With this cover, our *Find Minimum Crosstalk* is called.

The experimental result is shown in Table I and Table II. The column labeled *original* is the initial circuit optimized by *Espresso*. Column *Tien's* is the result of Tien's work [3]. Notice that in Tien's work, the total crosstalk effect of a circuit is minimized by grouping product terms. Column *ours* shows

Algorithm *Find_Minimum_Crosstalk*(*PLA*)
Begin
build *OGG* graph.
while(the number of vertices in *OGG* > 1)
Global_Transformation(PLA)
IO_Ordering(PLA)
Grouping_in_Long_Set(PLA)
PLA = interleaving(long, small)
Local_Transformation(PLA)
update the best solution.
update *OGG* graph.
end while
output the best solution.
End

Fig. 11. The *Find Minimum Crosstalk* algorithm

the result of our algorithm. In Table I, *total* and *max* represent the results of the total crosstalk effect and maximum crosstalk effect. The columns *TR* and *MR* are, respectively, the ratio of the total crosstalk effect and the maximum crosstalk effect produced by *Find Minimum Crosstalk* and Tien's grouping algorithm to those by *Espresso*. From Table I, we can see that the maximum crosstalk effect produced by our algorithm can be reduced by 48% while only 17% by Tien's work as compared to those of the original circuit. The total crosstalk effect is reduced by 73% by our algorithm while 79% by Tien's work. It is clear that our algorithm can greatly reduce the maximum crosstalk effect of PLA without increasing too much total crosstalk effect.

Table II compares the area overhead ratio. In Table II, the area cost of our algorithm is almost the same with original. In the case of *in2* and *max512*, the area cost by our algorithm is even better than the initial circuit optimized by *Espresso*. This is because our output grouping algorithm perturbs the initial circuit, hence gets rid of a local minima. Since the *Tien's* algorithm did not change the cover of a function, the number of product is the same as those in *original*.

VI. Conclusion

We have proposed a novel synthesis flow to minimize crosstalk of PLAs. Long set and short set interleaving technique reduces the overlapping length of PLAs. To further reduce the longest product-term length in *short*, grouping product terms in long set is used. Finally, synthesis techniques, *local transformation* and *global transformation*, to find a better cover for crosstalk reduction is proposed. The experimental results have demonstrated that our PLA synthesis methodology can effectively reduce the maximum crosstalk effect of PLA by 48%.

References

[1] A. Vittal, M. Marek-Sadowska, "Crosstalk reduction for VLSI", *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, pp. 290-298, vol. 16, i. 3, March 1997.

[2] K. W. Kim, U. Narayanan, S. M. Kang, "Domino logic synthesis minimizing crosstalk", *Proc. Design Automation Conference*, pp. 280-285, 5-9 June 2000.

TABLE I

RESULT OF CROSSTALK EFFECT

circuit	original		Tien's				ours			
	total	max	total	TR (%)	max	MR (%)	total	TR (%)	max	MR (%)
alu2	687	24	181	26.3	23	95.8	232	33.8	13	54.2
alu3	526	22	124	23.6	22	100.0	170	32.3	13	59.1
b10	2646	40	777	29.4	34	85.0	1046	39.5	23	57.5
b12	757	34	244	32.2	24	70.6	279	36.9	16	47.1
b3	12571	82	2036	16.2	68	82.9	2461	19.6	35	42.7
b9	886	33	85	9.6	28	84.8	95	10.7	17	51.5
bc0	8481	62	1678	19.8	46	74.2	2058	24.3	25	40.3
chkn	3135	60	245	7.8	48	80.0	241	7.7	30	50.0
dc2	582	20	180	30.9	17	85.0	247	42.4	14	70.0
ex7	886	33	85	9.6	28	84.8	95	10.7	17	51.5
gary	3015	40	1015	33.7	34	85.0	1339	44.4	24	60.0
ibm	13062	103	806	6.2	77	74.8	912	7.0	31	30.1
in0	3099	40	1015	32.8	34	85.0	1347	43.5	24	60.0
in2	4130	46	1008	24.4	36	78.3	1211	29.3	21	45.7
in7	1296	55	355	27.4	47	85.5	357	27.5	24	43.6
intb	3611	33	158	4.4	31	93.9	197	5.5	22	66.7
max1024	3550	25	432	12.2	21	84.0	666	18.8	14	56.0
max512	2239	23	340	15.2	21	91.3	464	20.7	13	56.5
newcond	74	20	15	20.3	15	75.0	22	29.7	13	65.0
newtpla	277	29	64	23.1	18	62.1	97	35.0	15	51.7
shift	3118	52	338	10.8	25	48.1	420	13.5	16	30.8
sqn	343	15	67	19.5	15	100.0	82	23.9	11	73.3
ts10	435	38	417	95.9	33	86.8	498	114.5	20	52.6
vg2	1977	56	241	12.2	50	89.3	398	20.1	31	55.4
vtx1	1434	56	223	15.6	50	89.3	306	21.3	34	60.7
x1dn	1434	56	223	15.6	50	89.3	306	21.3	34	60.7
x6dn	4227	81	439	10.4	69	85.2	545	12.9	20	24.7
x7dn	41194	144	688	1.7	81	56.3	692	1.7	28	19.4
x9dn	1586	58	279	17.6	53	91.4	396	25.0	36	62.1
average				20.8		82.5		26.7		51.7

TABLE II

RESULT OF AREA OVERHEAD

circuit	original	ours	
	product	product	ratio (%)
alu2	68	68	100.0
alu3	66	66	100.0
b10	100	100	100.0
b12	43	43	100.0
b3	211	211	100.0
b9	119	119	100.0
bc0	179	179	100.0
chkn	140	140	100.0
dc2	39	39	100.0
ex7	119	119	100.0
gary	107	107	100.0
ibm	173	173	100.0
in0	107	107	100.0
in2	136	135	99.3
in7	54	54	100.0
intb	631	631	100.0
max1024	274	274	100.0
max512	145	142	97.9
newcond	31	31	100.0
newtpla	23	23	100.0
shift	100	100	100.0
sqn	38	38	100.0
ts10	128	128	100.0
vg2	110	110	100.0
vtx1	110	110	100.0
x1dn	110	110	100.0
x6dn	82	82	100.0
x7dn	538	538	100.0
x9dn	120	120	100.0
average			99.9

[3] T. K. Tien, S. C. Chang, T. K. Tsai, "Crosstalk alleviation for dynamic PLAs", *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, pp. 1416-1424, vol. 21, i. 12, Dec. 2002.

[4] H. R. Jiang, Y. W. Chang, J. Y. Jou, "Crosstalk-driven interconnect optimization by simultaneous gate and wire sizing", *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, pp. 999-1010, vol. 19, i. 9, Sep. 2000.

[5] S. P. Khatri, R. K. Brayton, A. Sangiovanni-Vincentelli, "Cross-talk immune VLSI design using a network of PLAs embedded in a regular layout fabric", *Intl. Conf. Computer Aided Design*, pp. 412-418, 5-9 Nov. 2000.

[6] J. S. Wang, C. R. Chang, and C. Yeh, "Analysis and design of high-speed and low-power CMOS PLAs", *IEEE J. Solid-State Circuits Syst.*, vol. 36, i. 8, pp.1250-1262, Aug 2001.

[7] Fan Mo and R. K. Brayton, "River PLAs: A Regular Circuit Structure", *Proc. Design Automation Conference*, pp. 201-206, 10-14 June 2002.

[8] Y. B. Dhong, C. P. Tsang, "High speed CMOS POS PLA using predischarged OR array and charge sharing AND array", *IEEE Trans. Circuits and Systems*, pt. II, vol. 39, pp. 557-564, Aug. 1992.

[9] G. M. Blair, "PLA design for single-clock CMOS", *IEEE J. Solid-State Circuits*, pp 1211-1213, vol. 27, i. 8, Aug. 1992.

[10] S. P. Khatri, A. Mehrotra, R. K. Brayton, A. Sangiovanni-Vincentelli, R. H. J. M. Otten, "A novel VLSI layout fabric for deep sub-micron applications", *Proc. Design Automation Conference*, pp. 491-496, 21-25 June 1999.

[11] T. Sakurai and K. Tamaru, "Simple formulas for two and three dimensional capacitance", *IEEE Trans. Electron Devices*, pp.183-185, 1983.

[12] Giovanni De Micheli, "Synthesis and optimization of digial circuits", *McGRAW-HiLL*, 1994.

[13] E. M. Sentovich, K. J. Singh, L. Lavagno, C. Moon, R. Murgai, A. Saldanha, H. Savoj, P. R. Stephan, R. K. Brayton, A. Sangiovanni-Vincentelli, "SIS: A System for Sequential Circuit Synthesis", *Electronics Research Laboratory*, Memorandum No. UCB/ERL M92/41, 4 May 1992.