Early SEU Fault Injection in Digital, Analog and Mixed Signal Circuits: a Global Flow

R. Leveugle, A. Ammari
TIMA Laboratory
46, Avenue Félix Viallet - 38031 Grenoble Cedex – FRANCE - E-mail: Regis.Leveugle@imag.fr

Abstract

Fault injection techniques have been proposed for years to early analyze the dependability characteristics of digital circuits. Very few attempts have however been reported to perform the same task in analog parts. Furthermore, these attempts are all based on parametric variations. With the increasing number of mixed signal circuits, a unified approach becomes mandatory to globally validate the digital and analog parts, while taking into account real faults occurring in the field, e.g. SEUs. In this paper, a global analysis flow is proposed, based on a high-level model of the circuit. The possibility to inject transient faults in the different parts is discussed. The results obtained on a case study are reported to show the feasibility of the injection in analog blocks.

1. Introduction

The current evolution of the CMOS technologies increases the sensitivity of the circuits to their environment and consequently the probability of transient faults. Phenomena reported for years in the space environment, such as bit-flips due to the impact of particles in digital blocks (called Single Event Upsets, or SEUs), are becoming now observable even at the sea level, especially due to the impact of atmospheric neutrons. The need for integrated on-line detection or tolerance is therefore pervading everyday life applications such as mobile telecommunications or computing [1]. It becomes also mandatory to early analyze the functional consequences of the faults in order to (1) identify the significant nodes that should be protected in the circuit, so that overheads are kept to a minimum with respect to the actual protection needs, and (2) validate the efficiency of the implemented mechanisms. Such an early analysis must be performed as soon as possible in the design flow, and in any case before the fabrication of the first circuits, in order to reduce the costs and avoid time-consuming iterations.

Fault injection techniques have been proposed for years to analyze and/or validate the dependability characteristics of a circuit. Approaches aiming an early analysis have been proposed, based on the high-level modeling of the circuits and either simulation [2, 3, 4, 5, 6] or emulation [7, 8]. These approaches are typically based on VHDL models, and could easily be extended to Verilog models, but remain limited to digital parts. The main advantage is to be able to perform the analyses starting with the behavioral (or at least RTL) description of the circuit, and to refine the results along with the design refinement, down to the gate level. The main drawback of these approaches lies in the limitation to digital blocks.

Nowadays, analog and mixed signal (AMS) circuits are increasingly required in applications such as automotive, real-time control systems, communications or consumer electronics. The analog design and test methodologies are currently far behind their digital counterpart, and the analog blocks are therefore often the bottleneck when designing an AMS circuit. Similarly, analyzing the dependability of the circuit has only be done by injecting faults in the digital parts, that may not be sufficient in some cases since analog parts are also subject to transients. Indeed, approaches were proposed to harden some analog or mixed signal blocks to limit the effect of such transients, but the validation is generally based only on ad-hoc SPICE-like simulations performed on the block alone. The global analysis at the circuit or system level was not considered.

In [9], redundant structures are proposed to improve the reliability of analog-to-digital converters. These proposals are guided by a sensitivity analysis for alpha-particle induced transients. The analysis was performed at the transistor level, using the injection of currents whose equation is given by a double exponential model. The results show that the analog part of the converter can be more sensitive than the digital part. Such an analysis can be seen as equivalent to a dependability analysis at gate level in the digital parts, and can only be done quite late in the design flow (i.e. just before layout). Furthermore, the actual impact on the whole system of the erroneous behaviors of the converter can hardly be evaluated.

On the opposite, the proposal in [10] deals with the injection of faults in behavioral descriptions of analog blocks. Such a high-level description can be done in languages such as VHDL-AMS or Verilog-A and may allow a system-level analysis. However, injecting faults at the behavioral level is done by modifying the equations describing the behavior, i.e. by injecting parametric faults. Such faults can be representative of either process

1530-1591/04 $20.00 (c) 2004 IEEE

variations or circuit aging, but can hardly model the effect of transients due for example to particle hits.

An approach allowing a designer to globally evaluate, early in the design process, the response of an AMS circuit or system when transient faults occur is therefore lacking. The aim of this paper is to propose such an approach for SEU-like faults and to show results obtained on a test case.

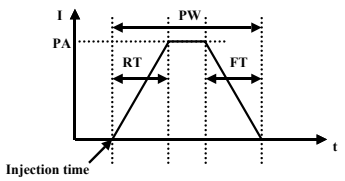
The targeted type of fault and its modeling is discussed in section 2. The existing digital analysis flow is then summarized in section 3 and the proposed flow for AMS circuits is presented in section 4. Section 5 discusses some results obtained on a test case.

2. Modeling of targeted faults

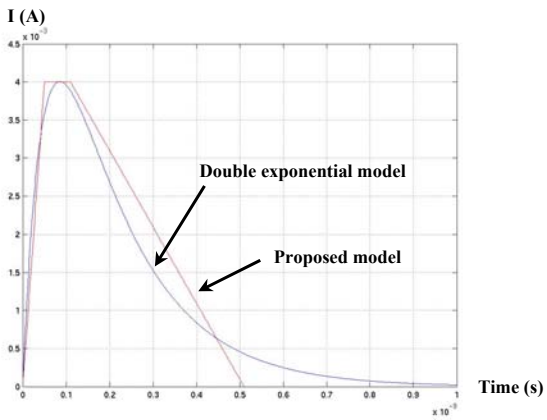
As mentioned in the introduction, the aim is to analyze the effects of actual transient faults occurring in the field, i.e. Single Event Upsets (SEUs) or Single Event Transients (SETs).

At the electrical level, a SET or a SEU corresponds to a current spike provoked by ionization, for example after a particle hits the circuit. When occurring in the combinatorial parts of a digital block, this current pulse creates a voltage variation (called SET) that may propagate through the gates until it is eventually captured (or not) in a flip-flop, potentially leading to one or more erroneous bits. When occurring directly in a flip-flop element, the current spike may produce an inversion of the element state (called SEU). The actual probability to latch a SET can only be evaluated very late in the design process, since it strongly depends on the propagation times in the combinatorial networks and its evaluation therefore requires the availability of the gate-level description with retro-annotation data. However, the consequence of both SETs and SEUs in a synchronous digital block can be modeled at the functional level by one or several bit-flip(s). In some cases, a higher level modeling can even be used, such as erroneous transitions in a finite state machine [11]. It is therefore possible to analyze the potential impact of SETs and SEUs by injecting bit-flips in the high-level description of a digital block, available very early in the design flow.

In the case of an analog block, the current spike cannot be modeled so simply. However, it is mandatory, from the practical point of view, to limit the complexity of the model in order to simplify the simulations and reduce the fault injection experiment duration. A double exponential model for the current pulses, as proposed in [12], is thus not suitable. We propose therefore to use a model of the current spike similar to the voltage pulse model used for SETs, but with more parameters. Figure 1(a) illustrates this model and shows the main parameters: injection time, pulse amplitude (PA), rising time (RT), falling time (FT) and pulse width (PW). The parameter values can be derived from the classical double exponential model, as illustrated in Figure 1(b), or they can be varied in a given interval during the fault injection experiments to study the sensitivity with respect to various events. Although this fault model remains at very low level, it can be used to perform injections on structural nodes in the high-level description of an analog block, by superposition of the current spike with the normal current at the target node. This will be detailed in section 4.



(a)



(b)

Figure 1: (a) Proposed modeling of the transient fault for analog blocks and (b) possible fit with the double exponential model.

3. Digital analysis flow

3.1. Steps of analysis

Figure 2 illustrates the main steps in a digital dependability analysis flow [11]. The initial circuit description can be either instrumented or used without any modification. In most cases, an instrumentation is done by transforming the VHDL code before synthesis and may use either saboteurs or mutants. This alternative is discussed in section 3.2. and the alternative without instrumentation (e.g., using simulator primitives) will not be considered further in this paper. The injection campaign can then be run using either simulation or emulation and the resulting traces are used either to classify the faults with respect to their impact on the behavior, or to generate a more complete model showing the error propagations in the circuit. During the campaign definition, the designer provides all the information required for the fault injection and the result analysis.

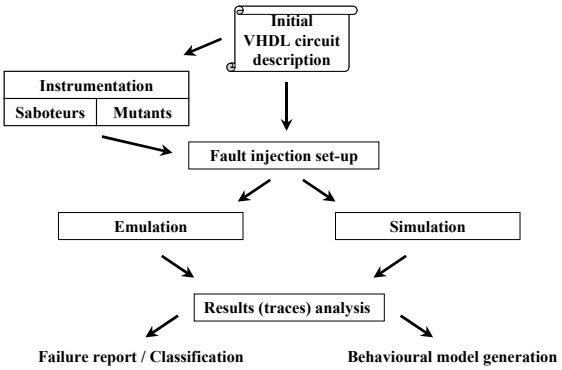


Figure 2: Main steps in the digital analysis flow [6].

3.2. Saboteurs and mutants

Two different approaches can be used to modify the initial description of the circuit. The first one consists in modifying the structure of the description by adding, between the existing blocks, some additional blocks able to insert some kinds of faults. These blocks were called **saboteurs** in [6]. Such modifications are conceptually quite easy and require only to modify some interconnections in the initial description. However, by consequence, the saboteurs can only inject faults on these interconnections and it is almost impossible to inject higher-level (behavioural) errors or to modify signals within the initial blocks, that is required for example to modify the value of memorised signals or variables. In such cases, some blocks in the initial description have to be directly modified, that is more difficult but much more powerful. In this case, the modified description of the block is called a **mutant**. The injection of bit-flips in high-level descriptions of digital blocks, as presented in section 2, uses such mutants [11].

4. AMS analysis flow

4.1. Extension of the digital flow

The goal of the proposal is to be able to inject transients in all the blocks of an AMS circuit, while making as few modifications as possible to the digital analysis flow.

A high-level description of the whole circuit is therefore assumed available. In our case, VHDL-AMS was chosen as the language for the initial description and the analog blocks are described in a mixed structural/behavioral style: the internal architecture of the block is specified by a hierarchical structural description, each basic sub-block being specified at the behavioral level.

A first modification in the previous flow is therefore of course to replace the VHDL (or Verilog) simulator by a mixed mode simulator. The emulation alternative is currently not considered. However, such an alternative may become practical in the future, on the basis of new mixed signal PLDs, such as the one recently introduced by Lattice Semiconductor.

In order to be compatible with the practices in digital design, the fault injections in the analog blocks should use either saboteurs or mutants. The high-level description of the basic analog sub-blocks is based on a set of equations that cannot easily be modified so that transients are accurately taken into account. On the opposite of the approach for digital parts, SEU-like faults must therefore be injected using saboteurs. Using a saboteur has also the advantage of a great flexibility for the current spike modeling. However, the injection is limited to interconnections between the sub-blocks ; the number of possible injection targets therefore directly depends on the architectural decomposition of the analog block. Avoiding this limitation is a clear subject for further work. Of course, parametric fault injections can still be done, when significant, in the basic sub-blocks described at the behavioral level.

Since the saboteur description can be made available in a library, the instrumentation of the analog blocks is very easy. However, the designer must specify (1) the range of the parameters for the pulse specification (defined in section 2) and (2) the injection times. Specifying the injection times is more complex for analog blocks than for digital ones, since the exact injection time (and not only the injection cycle with respect to the system clock) may have a noticeable impact on the fault effects, even when a behavioral simulation of the digital part is performed.

The analysis of the results can use the module available in the digital flow if only digital nodes are monitored during the experiments. In case analog nodes are also monitored, it may be necessary to define an additional tolerance on the values, in order to avoid non significant error identifications.

The resulting flow is illustrated in Figure 3.

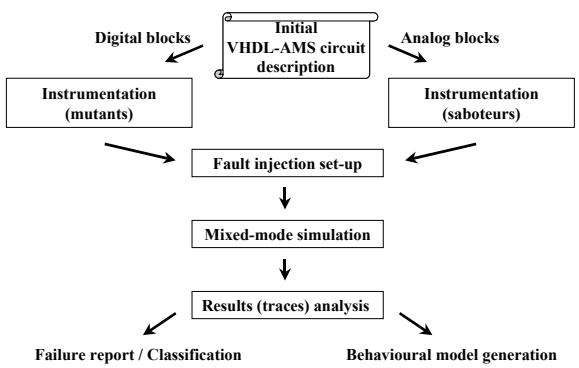


Figure 3: Main steps in the proposed AMS analysis flow.

4.2. Saboteur generic model

The description of the saboteur can be made fully generic. Figure 4 shows an example of generic saboteur described in VHDL-AMS and using the parameters defined in section 2. With such a description, current pulses can be injected on nodes specified as "current quantities" by using a current summation on the node. The duration of the current pulse (PW) is in this example controlled through the duration of the external injection control signal.

```
library Disciplines, IEEE;
use Disciplines.ELECTROMAGNETIC_SYSTEM.all;
use IEEE.math_real.all;

entity GenCur is
  generic ( RT: real;
            FT: real;
            PA: real );
  port ( terminal out_cur : electrical;
         signal inj: in bit);
end entity GenCur;

architecture GenArch of GenCur is
  quantity out_current through out_cur;
  signal intI: real:=i1;
  begin
    p: process(inj)
    begin
      intI <= 0;
      if inj='1' then
        intI <= PA;
      end if;
    end process;
    out_current == intI'ramp(RT,FT);
end GenArch;
```

Figure 4: Example of generic description in VHDL-AMS of a saboteur for current pulse injection.

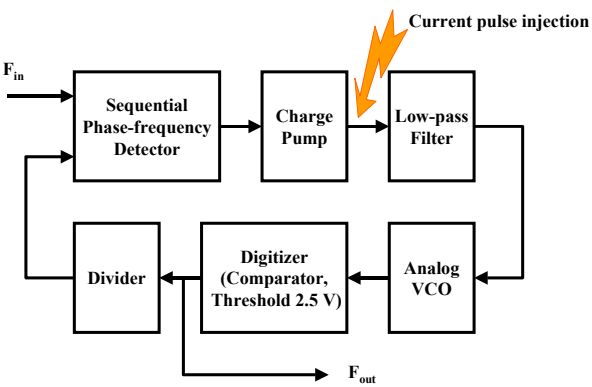


Figure 5: Hierarchical structure of the PLL block.

5. Results on a test case

5.1. Description of the test case

Experiments were carried out using the mixed-mode simulator ADVance-MS from Mentor Graphics. The circuit used as test case included a PLL (phase-locked loop) analog block generating the clock signal of a digital block. The goal of this paper is to demonstrate the feasibility of transient fault injection in the analog parts ; we will therefore focus here on the injections in the PLL block. This block was similar to the frequency synthesizer described in [13] and its hierarchical structure is illustrated in Figure 5. Each sub-block was specified at the behavioral level. The input frequency was 500KHz. The period of the generated clock was 20 ns (50 MHz).

5.2. Results and discussion

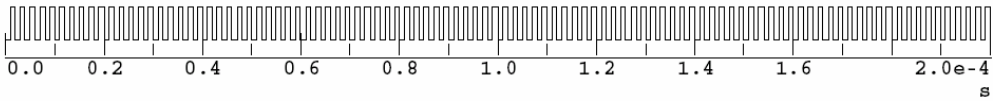
The fault injections reported here were done by inserting the saboteur output at the input of the low-pass filter (i.e., at the output of the charge pump). Some results are illustrated in Figure 6, with an injection at 0.17 ms, after the VCO is locked. The characteristics of the current pulse were RT=100 ps, FT=300 ps, PW=500 ps, PA=10 mA. Let us notice that 10 mA is a typical amplitude value; larger amplitudes have been reported [14].

As can be seen on the figure, the current pulse injected during a very short time (2.5% of the generated clock period), has an impact on the filter output during a much larger time. This results in a clock frequency on the F_{out} signal that is perturbed during a large number of cycles and not only during one cycle, as might be expected from the short duration of the fault. Identifying the number of consecutive cycles during which the single fault can generate errors is an important result, since it allows the designer to refine the dependability analysis in the digital part, taking into account multiple errors when necessary.

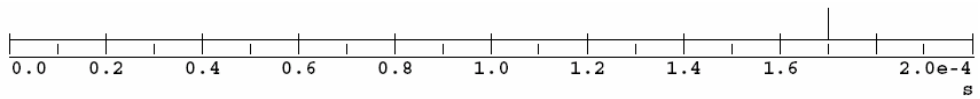
Let us notice that, in the particular case studied, the variation in the clock frequency may not directly induce logical errors in the simulation results of the digital part, if described at the behavioral level. However, the variation could eventually induce errors on the critical path in the manufactured circuit, so the early dependability analysis has to take into account this potential multiplicity of errors generated by a single event. Also, for other injection locations or other types of blocks, the impact of the fault could directly imply a logic error (e.g. spurious edge on the clock, or modified digital output). In these cases, the propagation of the logic error would directly be observed in the behavioral simulations of the complete mixed signal circuit.

Figure 7 shows results obtained for the same fault injection experiment, using either a double exponential shape or the proposed model for the current pulse. It can be seen that the results are very similar, although the numeric values are slightly different. Figure 8 illustrates results obtained with several current pulse definitions; the amplitude and length of the pulse have clearly a cumulative effect for this example. Such results may allow the designer to identify the type of particles the circuit will be sensitive to.

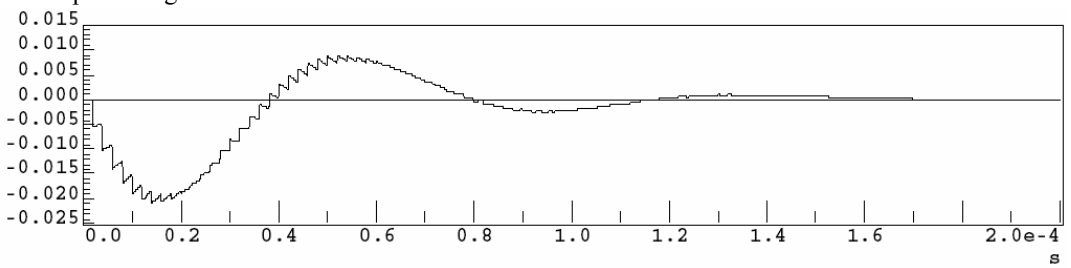
Input signal (500 KHz)



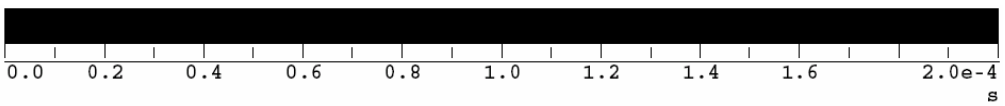
Injection control signal



Nominal input voltage of VCO



Generated clock signal (F_{out})



Input voltage of VCO with fault injection

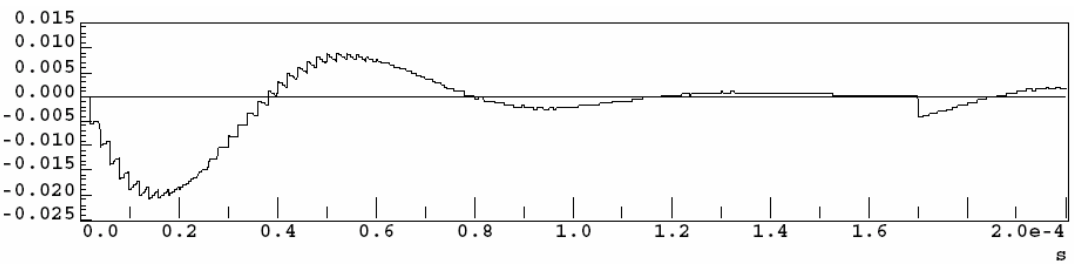
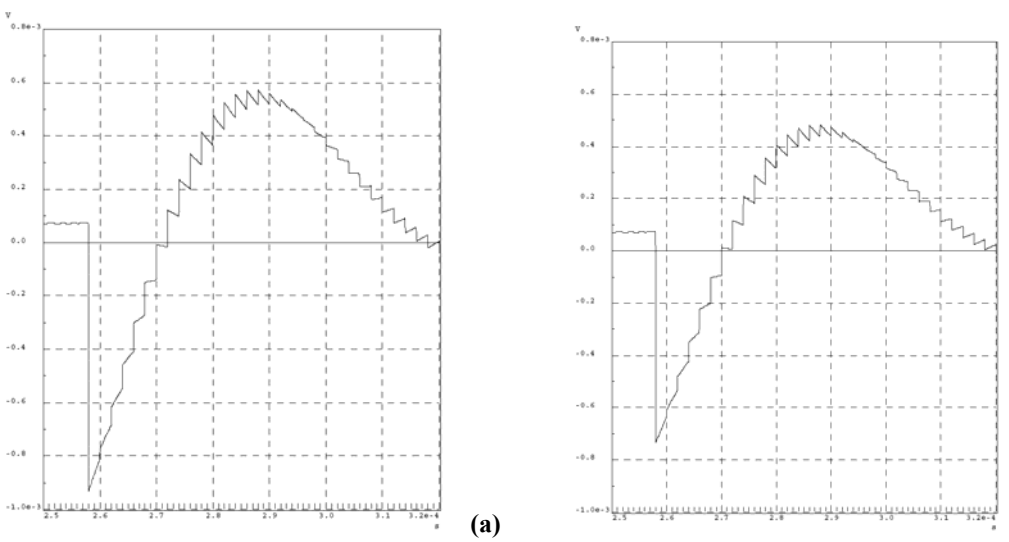
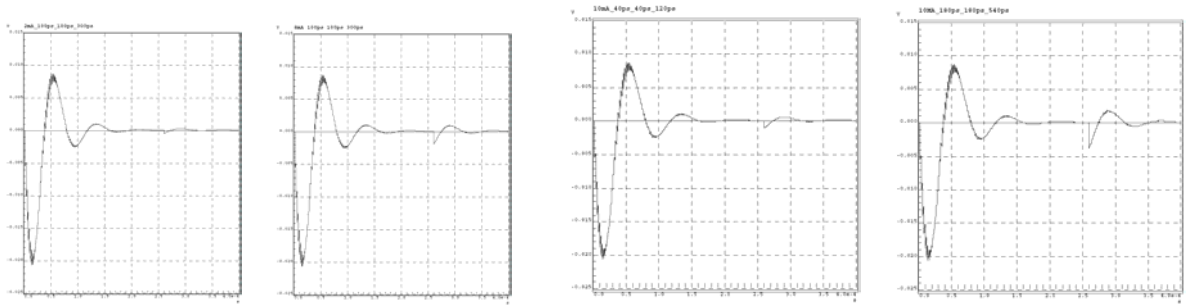


Figure 6: Fault injection results in the PLL block.



(a) **(b)**

Figure 7: Results obtained on the VCO input for two injections at the same time, using either the double exponential model (a) or the model proposed in Figure 1b (b) to model the current pulse.



(2 mA, 100 ps, 100 ps, 300 ps) (8 mA, 100 ps, 100 ps, 300 ps) (10 mA, 40 ps, 40 ps, 120 ps) (10 mA, 180 ps, 180 ps, 540 ps)

Figure 8: VCO input signal for several sets of parameters (PA, RT, FT, PW) defining the current pulse injected on the filter input.

6. Conclusion

The test case demonstrated both the feasibility to provide a unified flow for digital and analog blocks and the interest of the approach when early analyzing the effect of transients on the behavior of AMS circuits.

The PLL function was chosen here as demonstrator, but the interest of the approach could be still higher when analyzing the impact of faults in functional blocks including both analog and digital circuitry, e.g. analog to digital converters. Our future research includes the analysis of such blocks using the flow proposed in this paper. Comparisons between results obtained on behavioral models and results obtained on lower level descriptions are also planned.

References

[1] R. Leveugle, "Automatic modifications of high level VHDL descriptions for fault detection or tolerance", Design, Automation and Test in Europe Conference (DATE), March 4-8, 2002, pp. 837-841

[2] G. C. Cardarilli, F. Kaddour, A. Leandri, M. Ottavi, S. Pontarelli, R. Velazco, "Bit-flip injection in processor-based architectures: a case study", 8th IEEE International On-Line Testing workshop, Isle of Bendor, France, July 8-10, 2002, pp. 117-127

[3] L. Berrojo, I. Gonzalez, F. Corno, M. Sonza-Reorda, G. Squillero, L. Entrena, C. Lopez, "New techniques for speeding up fault-injection campaigns", Design, Automation and Test in Europe Conference (DATE), March 4-8, 2002, pp. 847-852

[4] F. Vargas, A. Amory, R. Velazco, "Estimating circuit fault-tolerance by means of transient-fault injection in VHDL", 6th IEEE International On-Line Testing workshop, Palma de Mallorca, Spain, July 3-5, 2000, pp. 67-72

[5] J. Gracia, J. C. Baraza, D. Gil, P. J. Gil, "Comparison and application of different VHDL-based fault injection techniques", "The IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems, San Francisco, California, USA, October 24-26, 2001", IEEE Computer Society Press, 2001, pp. 233-241

[6] E. Jenn, J. Arlat, M. Rimen, J. Ohlsson, J. Karlsson, "Fault injection into VHDL models: the MEFISTO tool", 24th Symposium on Fault-Tolerant Computing (FTCS), 1994, pp. 66-75

[7] R. Leveugle, "Fault injection in VHDL descriptions and emulation", "The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Yamanashi, Japan, October 25-27, 2000", IEEE Computer Society Press, Los Alamitos, California, 2000, pp. 414-419

[8] P. Civera, L. Macchiarulo, M. Rebaudengo, M. Sonza Reorda, A. Violante, "Exploiting FPGA-based techniques for fault injection campaigns on VLSI circuits", "The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, San Francisco, California, USA, October 24-26, 2001", IEEE Computer Society Press, Los Alamitos, California, 2001, pp. 250-258

[9] M. Singh, I. Koren, "Reliability enhancement of analog-to-digital converters (ADCs)", "The IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems, San Francisco, California, USA, October 24-26, 2001", IEEE Computer Society Press, 2001, pp. 347-353

[10] P. R. Wilson, Y. Kilic, J. N. Ross, M. Zwolinski, A. D. Brown, "Behavioural modeling of operational amplifier faults using VHDL-AMS", Design, Automation and Test in Europe Conference (DATE), March 4-8, 2002, pp. 1133

[11] R. Leveugle, K. Hadjiat, "Multi-level fault injections in VHDL descriptions: alternative approaches and experiments", Journal of Electronic Testing: Theory and Applications (JETTA), Kluwer, October 2003

[12] G. C. Messenger, "Collection of charge on junction nodes from ion tracks", IEEE Transactions on Nuclear Science, 1982, pp. 2024-2031

[13] B. Antao, F. El-Turky, R. Leonowich, "Behavioral modeling phase-locked loops for mixed-mode simulation", Analog Integrated Circuits and Signal Processing, vol. 10, 1996, pp. 45-65

[14] F. L. Yang, R. A. Saleh, “Simulation and Analysis of Transient Faults in Digital Circuits” IEEE Journal of Solid-State Circuits, vol. 27, no. 3, March 1992, pp. 258-264