

# Identification and Modeling of Nonlinear Dynamic Behavior in Analog Circuits

Xiaoling Huang                      H. Alan Mantooth  
xxh02@engr.uark.edu              mantooth@engr.uark.edu  
Department of Electrical Engineering  
University of Arkansas, Fayetteville, AR 72701 USA

## Abstract

*This paper presents a new approach for identifying nonlinear dynamic behavior in analog circuits. The approach facilitates the creation of models that more accurately reflect the dynamic behavior of a circuit. It has been used in a fully automated, behavioral modeling tool, Ascend, that starts from the netlist description of the circuit and generates differential algebraic equation (DAE) based behavioral models. The underlying modeling approach is overviewed to provide a context for this research. Some demonstrative test results illustrate the effectiveness of the new method.*

## 1. Introduction

As the complexity and performance criteria of analog and mixed-signal systems are steadily increased, it becomes crucial for design engineers to be able to perform rapid higher-level simulations achieved by using behavioral models. Research into behavioral modeling techniques and algorithms has continued since the 1970s. While things have matured nicely in the modeling of linear circuits and systems, developing modeling methodologies for circuits with nonlinearities remains a challenge. Recently, several approaches of behavioral model generation for nonlinear circuits have been presented.

One of the efforts involves the creation of behavioral models from measurement data [1-3]. While these methods don't strictly adhere to the premise of starting from the circuit netlist, they have nonetheless been proven to be valuable for modeling nonlinearities associated with diodes and FETs. Symbolic analysis has for the past two decades focused intensely on linear systems, but recently work has begun on nonlinear circuits as well [4]. Roychowdhury [5,6] and Phillips [7,8] have each

described projection-based methods that can be extended to weakly nonlinear circuits. In [9] Li proposes a reduced-order macromodel to represent the nonlinearities of RF/analog circuits at the system level.

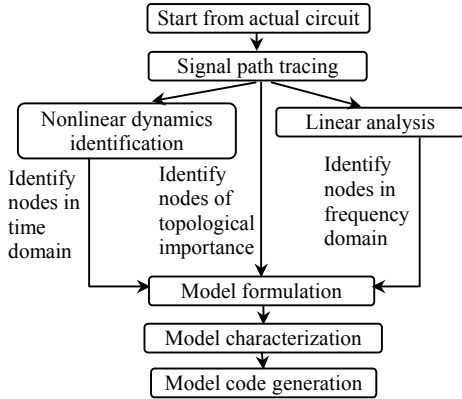
In [10], a modeling procedure was first described that enabled the modeling of nonlinear behavior. Compared to other behavioral modeling methods, this is a bottom-up behavioral modeling approach that doesn't require a pre-defined template for the topology of the model. Instead, the approach automatically produces a model structure based on critical roots, signal paths, and a set of nodes. Currently, the behavioral modeling procedure has been fully automated into the Ascend tool within the Paragon behavioral modeling environment [11], [12].

The main contribution of this paper is a technique for effectively identifying nonlinear dynamical behavior in analog circuits, which has been incorporated into Ascend. While the modeling approach is detailed in [10,13], this paper will focus on the identification and modeling of nonlinear dynamics. The organization of the paper is as follows. Section 2 gives a brief overview of the modeling procedure. In Section 3, the technique for identifying nonlinear dynamical behavior is described in detail, and some illustrative results are presented. Finally, a full modeling example is used to demonstrate nonlinear dynamics identification and the associated modeling approach to produce accurate, nonlinear behavioral models in Section 4.

## 2. Modeling procedure

The Ascend automated modeling procedure, illustrated in Fig. 1, starts from the netlist description of the circuit and generates DAE based behavioral models. The basic idea behind this approach is to analyze the original circuit for a) signal path information, b) linear frequency response, and c) nonlinear time-domain response to identify a subset of nodes in the original circuit. Each identified node is physically represented in the model by a DAE derived by Kirchhoff's Current Law (KCL), the entire set of which forms a reduced set from that of the original circuit. Each DAE can be represented by a

† This work was sponsored by DARPA/MTO NeoCAD Program under Grant No. N66001-01-1-8919, by Office of Naval Research under Subaward No. USC 01-636, and by an NSF CRCD award (EEC-0088011).



**Fig. 1. Ascend behavioral modeling procedure.**

collection of elements such as voltage-controlled current sources (VCCSs) and linear and nonlinear passives.

A signal-path tracing (SPT) algorithm [13] is applied at the first step to categorize the nodes in the circuit into two groups. Any node in the original circuit that falls into any fully traced input-output signal path is referred to as a signal-path node. All others are non-signal-path nodes. Only signal-path nodes are used in the derivation of the final model.

The second step in the modeling procedure is to identify a subset of the signal-path nodes to be modeled. These nodes are chosen based on three scenarios. The first subset is identified based on frequency domain criteria. The second subset is those nodes that are important strictly from a nonlinear dynamic perspective in time domain. The third subset is the signal path nodes that may be required from a topological standpoint.

The linear analysis identifies a subset of nodes to be modeled in frequency domain. Using root sensitivities, the root localization (RL) algorithm [12] is employed to numerically determine when poles and zeros are a localized phenomenon. When a root is largely dependent on elements connected to a single node or a coupled pair, it will be hereafter referred to as topologically *localized*. In contrast, other poles and zeros that are not dominated by elements at a single node or coupled pair, but rather are a function of many elements connected in various parts of the circuit, will be referred to as *delocalized*.

The nonlinear dynamical nodes are identified by performing large-signal time-domain and DC sweep analyses of the original circuit. Identification is based on the properties of the nodal currents in response to stepwise voltage injections at signal path nodes. The identification method will be described in detail in Section 3.

Topologically important nodes include input nodes, output nodes and signal-mixing nodes where signals are algebraically combined. Signal-mixing nodes can be identified by performing comparisons between the traced signal paths.

Model formulation creates an overall structure of the model. Once all of the nodes are identified, the model of each identified node is formed by a symbolic summation of currents at that node. This produces a set of physically modeled nodes functionally related to each other through VCCSs. The dependencies of these controlled sources are derived from the signal paths.

Model formulation essentially depends on two factors: the identified nodes and the roots to be modeled. The circuit's roots can be modeled in one of two ways: linearly or nonlinearly. Modeling a root linearly means the root value will be constant and not sensitive to changes in operating conditions. This representation is simply a linear transfer function. Modeling roots "nonlinearly" refers to the fact that the nonlinear static and dynamic characteristics of the root are accurately captured such that the model is valid for all operating conditions. Only localized roots are modeled nonlinearly in this approach by modeling the nodes to which the roots are localized.

While the modeling potential of both the nonlinear static and dynamic behaviors have been established by the model formulation, model accuracy depends on the characterization process. Model characterization includes the extraction of data tables used to represent the controlled current sources in the model and the calculation of passive elements used in the physically modeled nodes. The nonlinear data tables combined with the nonlinear passives connected to the nodes provide a reasonable way of modeling nonlinear behaviors identified in the circuit.

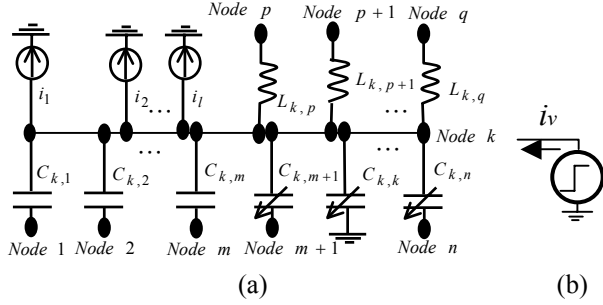
The model code generation step in Fig. 1 utilizes a module in PARAGON that generates the behavioral model in multiple languages including VHDL-AMS and MAST [14-16].

### 3. Identification of nonlinear dynamics

#### 3.1 Theoretical basis for nonlinear dynamics identification

A general node in an analog circuit can be physically represented as shown in Fig. 2 (a). This node may have resistors, capacitors, inductors, and VCCSs. The inductors are typically circuit elements as opposed to either parasitics or components of a device model, if present at all, and are treated as linear in this development. The resistors are not explicitly shown in Fig. 2 (a), but are included in the current sources. The VCCS is not only a function of node voltages elsewhere in the signal paths, but also the voltage of the node to which it is connected. In this way a nonlinear resistance is represented as part of the controlled source, since the current into the node depends on the voltage across it. The VCCSs are used to represent the linear and nonlinear static behavior (DC

behavior) of the node. The linear capacitors and inductors and nonlinear capacitors are connected to the node to represent the dynamic (linear and nonlinear) behavior.



**Fig. 2. (a) A physically represented node. (b) A step voltage source.**

If the node  $k$  shown in Fig. 2 (a) is excited with a fast rising transient (a step voltage source as shown in Fig. 2 (b)) where the rising edge is described as

$$\frac{dV_k}{dt} = a \quad (1)$$

where  $a$  is a constant, the current through the voltage source can be represented as

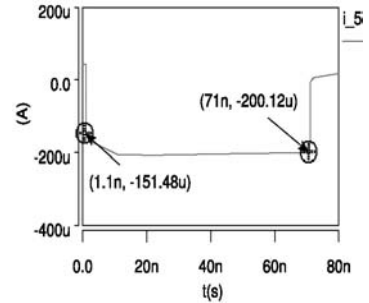
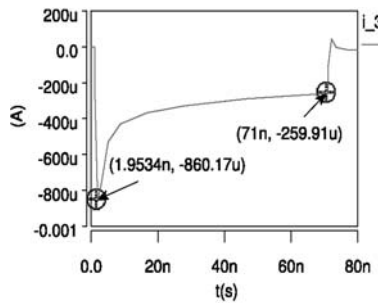
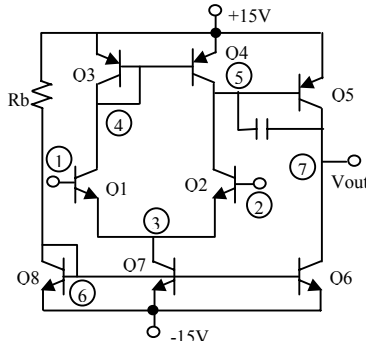
$$i_v = \sum_{j=1}^l i_j + C_{leq} \frac{dV_k}{dt} - \sum_{j=1}^m C_{k,j} \frac{dV_j}{dt} + \frac{d(C_{neq} \cdot V_k)}{dt} - \sum_{j=m+1, j \neq k}^n \frac{d(C_{k,j} \cdot V_j)}{dt} + \sum_{j=p}^q \frac{1}{L_{k,j}} \int V_k dt - \sum_{j=p}^q \frac{1}{L_{k,j}} \int V_j dt \quad (2)$$

where  $k > m$  is assumed,  $i_1, i_2, \dots, i_l$  represent the static current contributions to node  $i$  via transistors, resistors,

etc.  $C_{leq} = \sum_{j=1}^m C_{k,j}$  and  $C_{neq} = \sum_{j=m+1}^n C_{k,j}$  are the total

linear and total nonlinear capacitance at node  $k$ , respectively.  $C_{k,j}$  are the coupling capacitances between node  $k$  and other nodes.  $L_{k,j}$  are the inductances between node  $k$  and other nodes. The indices  $l$  and  $m$  are the number of VCCSs and linear capacitors at node  $k$ , respectively. The difference  $n-m$  is the number of nonlinear capacitors, and  $q-p$  is the number of inductors.

If the static terms are removed and the voltages at other nodes are held constant, Eq. (2) can be simplified and the resulting  $i_v$  is the dynamic current



**Fig. 3. (a) Schematic of a bipolar op amp. (b) Dynamic current at node 3. (c) Dynamic current at node 5.**

$$i_{v\_dynamic} = C_{leq} \frac{dV_k}{dt} + \frac{d(C_{neq} \cdot V_k)}{dt} - \sum_{j=m+1, j \neq k}^n \frac{d(C_{k,j} \cdot V_j)}{dt} + \sum_{j=p}^q \frac{1}{L_{k,j}} \int V_k dt - \sum_{j=p}^q \frac{1}{L_{k,j}} \int V_j dt \quad (3)$$

Substituting for  $\frac{dV_k}{dt} = a$ , and assuming the initial voltage at node  $k$  is zero, the dynamic current is given by

$$i_{v\_dynamic} = C_{leq} \cdot a + \frac{d(C_{neq} \cdot V_k)}{dt} - \sum_{j=m+1, j \neq k}^n \frac{d(C_{k,j} \cdot V_j)}{dt} + \sum_{j=p}^q \frac{1}{L_{k,j}} \cdot \frac{1}{2} a t^2 - \sum_{j=p}^q \frac{1}{L_{k,j}} V_j \cdot t \quad (4)$$

Furthermore, the currents due to inductors can be removed because they can be calculated exactly. Thus, the capacitive component of the dynamic current is obtained

$$i_{v\_dynamic\_cap} = C_{leq} \cdot a + \frac{d(C_{neq} \cdot V_k)}{dt} - \sum_{j=m+1, j \neq k}^n \frac{d(C_{k,j} \cdot V_j)}{dt} \quad (5)$$

It can be observed from Eq. (5) that

- Linear dynamic behavior is dominant at the node if  $i_{v\_dynamic\_cap}$  is approximately constant meaning the second and third terms in Eq. (5) are negligible.
- Nonlinear dynamic behavior is dominant at the node if the variation of  $i_{v\_dynamic\_cap}$  is relatively large.

The current  $i_{v\_dynamic\_cap}$  can be calculated by performing transient and DC sweep analyses of the circuit.

A criterion is specified for evaluation of the dynamic current to determine whether or not nonlinear dynamics are significant and thus modeled at the node. The magnitude of the normalized derivative of the dynamic current is defined as

$$deri = \left| \frac{di}{dt} \cdot \frac{t}{i} \right| \quad (6)$$

In the time period  $[T_a, T_b]$ , the mean magnitude of normalized derivatives can be calculated using

$$deri\_mean = \frac{\sum_{k=1}^{n-1} \left| \frac{i_{k+1} - i_k}{t_{k+1} - t_k} \cdot \frac{t_{k+1}}{i_{k+1}} \right|}{n-1} \quad (7)$$

where  $i_k$  is the  $k$ th sample current at time  $t_k$ . The index  $n$  is the number of sampling points; usually 500 points are used in order to obtain an acceptable accuracy. If the

mean magnitude of normalized derivatives is close to zero, the dynamic current is approximately constant, which leads to the conclusion that linear dynamic behavior is dominant at the node. Otherwise, if the mean magnitude of normalized derivatives of dynamic current at a node exceeds a user-specified threshold, the node will be identified for nonlinear dynamics. A value of 0.1 is typically used as a threshold, which has proven to be acceptable for model accuracy.

### 3.2 Experimental results

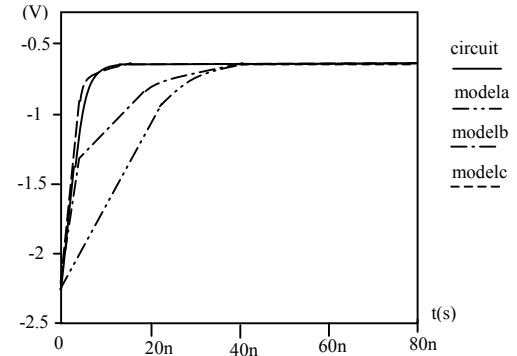
**Table 1. Experimental results for identification of nodes based on nonlinear dynamics**

Circuits	Total number of nodes	non-signal-path nodes	signal-path nodes	nonlinear nodes
HDR Op Amp	16	4	12	2
HUSS Op Amp	14	5	9	1
BJT Op Amp	9	3	6	1
741 Op Amp	25	9	16	5
Comparator	15	5	10	2
Gilbert Mixer	13	4	9	0

To demonstrate and validate the efficacy of the new method on nonlinear dynamics identification, a bipolar op amp with NPN input devices (Fig. 3 (a)) was investigated. Nodes 1-5 and 7 were identified to be signal path nodes. A rise time is chosen such that the continuous-time Fourier Transform of the input signal has a -3 dB frequency equal to ten times the unity gain frequency of the circuit (a conservative estimate). The rise time of the step voltage was determined to be 70 ns, based on a unity gain frequency of 1 MHz. The magnitudes of the excitation signals were determined when the voltage of one input changed from -12V to +12V while the other input was connected to ground. The dynamic currents at nodes 3, 4, 5 and 7 were extracted. For illustration, the dynamic currents at node 3 and node 5 are shown in Fig. 3 (b) and Fig. 3 (c). It is obvious that the variation of the dynamic currents at node 3 is much larger than that at node 5. Based on the calculation of the deviation ratios and relative ratios, node 3 was identified to be modeled based on nonlinear dynamics.

The method has been applied to a range of circuits, such as amplifiers, comparators and mixers. Both MOS and bipolar technologies were investigated. The experimental results for some benchmark circuits are shown in Table 1. In most cases, one or two signal-path nodes were identified as possessing significant nonlinearities. However, one example illustrates that this is not always the case. The Gilbert cell mixer behavior was dominated by linear capacitive effects. Simulation results of these circuits indicate a dramatic improvement in model accuracy for high-speed switching by including these effects. This is illustrated in Fig. 4 where the dotted curves indicate three model results as compared to the

original comparator circuit of Table 1. The model curves are for the cases of a) no nonlinear effects, b) one of two nonlinear effects, and c) two identified nonlinear dynamic effects (best-fit).



**Fig. 4. Source-coupled voltage waveforms of the comparator and several versions of the model.**

### 4. A modeling example

Fig. 5 is the schematic of a high dynamic range CMOS op amp. It consists of two differential amplifiers and a completely symmetrical output structure intended to reduce distortion.

The traced signal paths are shown in Fig. 6. Nodes 1-8, 12, 13, 20, and 22 were determined to be signal path nodes. Nodes 5, 8, 12, 13 and 20 were discovered to be signal-mixing nodes by comparing these signal paths.

There were a total of 21 roots (poles and zeros) in the circuit, which were calculated by the linear analysis. The RL algorithm was applied and revealed that only 4 poles and 1 zero were localized in the frequency range of interest (i.e., one decade above the unity-gain frequency). Referring to Fig. 5, the poles at 107 kHz, 162 kHz and 459 kHz were localized to nodes 4, 22 and 5, respectively. It also revealed that the low-frequency pole at 29 Hz and the zero at 307 kHz were both localized to the capacitively coupled nodes 20 and 22. Thus, four nodes (4, 5, 20 and 22) were identified in frequency domain by the RL algorithm [12].

Based on the method described in Section 3, the dynamic current of each signal path node was extracted. As shown in Table 2, nodes 3 and 6, were identified based on nonlinear dynamics because their mean magnitude of normalized derivatives exceeded the user-specified tolerances, which was specified to be 0.1.

The degree of accuracy required of the model determines the model complexity. But for speed considerations, the simpler the model the better it will perform. It is desirable that the number of the nodes is minimized for a given level of accuracy. For this op amp, besides two inputs and the output, three identified nodes (nodes 3, 6 and 20) were selected. In order to represent

the nonlinear dynamic behavior of the circuit, nodes 3 and 6 are physically modeled. The movement with changing operating conditions of the dominant pole and the localized zero was modeled by selecting nodes 20 and 22. Other non-dominant poles and zeros were represented by linear transfer functions in the model. The selection of these nodes has been demonstrated to be sufficient for model accuracy as shown in the following. A rigorous, algorithmic method for choosing a subset of identified nodes to be modeled is still under investigation.

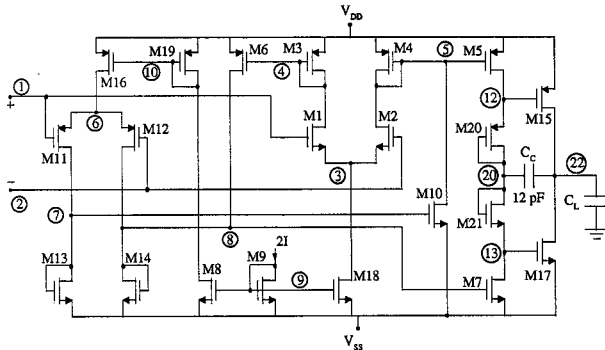


Fig. 5. Schematic of CMOS op amp.

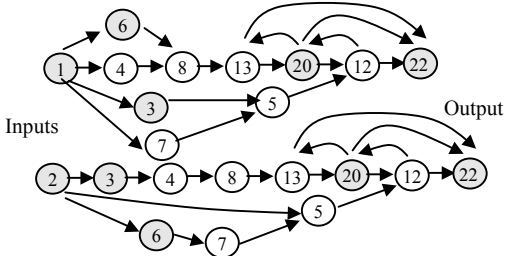


Fig. 6. Signal paths of op amp.

Table 2. Nonlinear dynamics identification result of op amp

Node Name	Mean Magnitude of normalized Derivatives
3	5.317e-01
4	2.477e-02
5	1.910e-02
6	1.063e-01
7	2.368e-02
8	4.313e-02
12	6.483e-02
13	2.719e-02
20	1.294e-02
22	4.924e-03

The behavioral model topology was formulated based on the nodes to be modeled [13]. A schematic version of the topology is shown in Fig. 7, where  $V_1$  and  $V_2$  are the inputs, and  $V_{22}$  is the output. The inputs control the device currents (drain or source currents of M1, M2, M18, M11, M12, M16) of the two differential pairs, which are currents into nodes 3 and 6.  $C_{T1}$  and  $C_{T2}$  are nonlinear capacitors representing nonlinear dynamics. At node 20 and 22, a single multidimensional controlled-current

source was used to model the static current contribution to each node. The dependencies of these controlled sources were derived from the signal paths. Four differential equations were formulated based on this model topology. The number of differential equations in this modeling methodology is largely decreased compared to [4], in which 5 differential equations are required for just a differential pair.

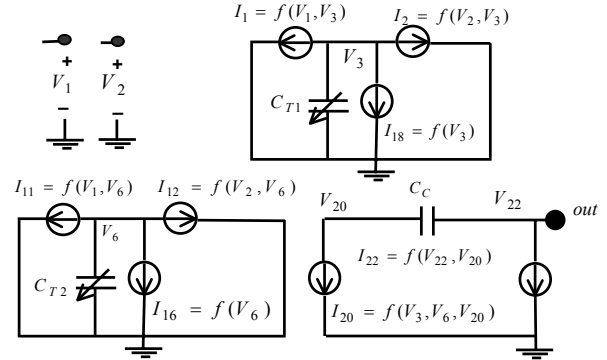
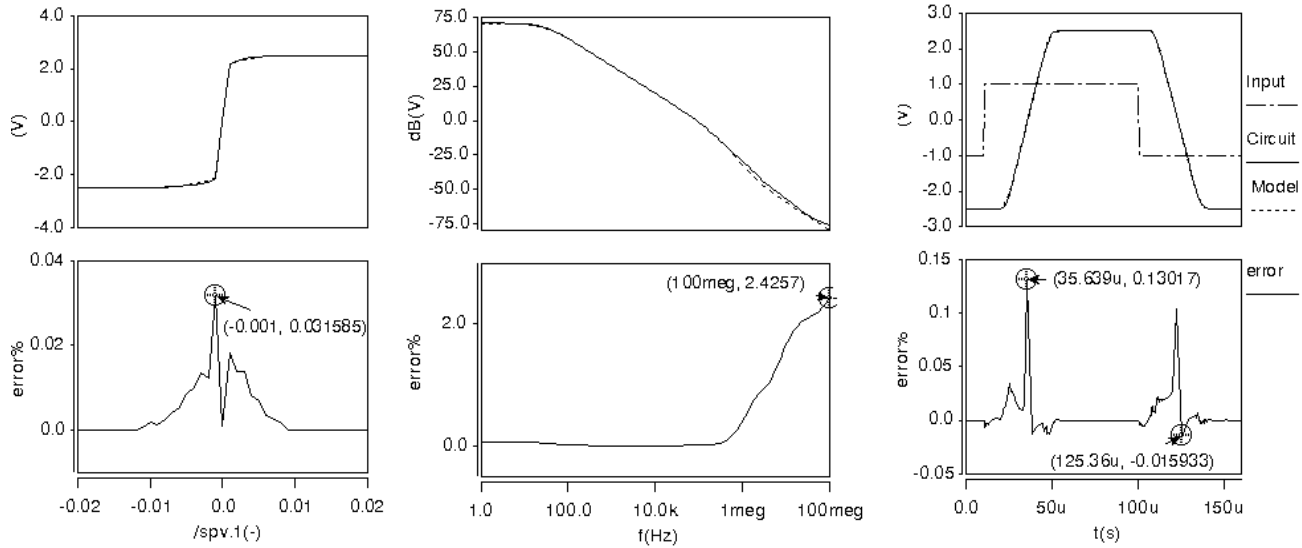


Fig. 7. Schematic representation of the model.

The computation cost during model creation is determined by the simulations performed on the original circuit. Consequently, the model creation time mainly depends on the number of tables, the dimension of tables and the number of points in the tables. It took about 30 minutes to create the model for this op amp on a Pentium 4 machine. The plots in Fig. 8 are obtained from simulation of the behavioral model and the circuit. The characteristics of the model, represented by the dashed lines in all plots, accurately match those of the circuit, represented by the solid lines. The lower plots in Fig. 8 are the percent error of the model compared to the original circuit for each simulation. The model exhibited speedup factors of about 10 with accuracies better than 2.5% as indicated in Fig. 8. All simulations were performed using Saber.

## 5. Conclusion

This paper described a new method for identification of nonlinear dynamic behavior in analog circuits. The method has been incorporated into an existing bottom-up behavioral modeling tool Ascend, which generates behavioral models based on the model order reduction achieved in terms of reduced nodes/roots modeling. A subset of nodes in the original circuit is identified for modeling nonlinear dynamics by the developed identification technique. Results indicate the identification method is reliable over technology and circuit type. A signal-path tracing algorithm and a linear root localization algorithm have been employed to identify two other subsets of nodes; those that are important topologically and those in the frequency domain, respectively.



(a) DC transfer curves      (b) AC frequency response      (c) Large-signal transient response  
**Fig. 8. Simulation results of op amp and model.**

Improvements in simulation times that typically range from 10-30x have been achieved with accuracies from 1-10% for circuit performance measures in the time and frequency domains. Future research work includes more efficient data representation suitable for model optimization and merger of this numerical method with symbolic analysis for model generation. The incorporation of symbolic analysis may make it possible to create more flexible parametric models.

## 6. References

- [1] D. E. Root, M. Pirola, S. Fan, W. J. Anklam and A. Cognata, "Measurement-based large-signal diode modeling system for circuit and device design," *IEEE Trans. Microwave Theory and Techniques*, vol. 41, pp. 2211-2217, Dec. 1993.
- [2] D. Schreurs, J. Wood, N. Tuffillaro, D. Usikov, L. Barford and D. E. Root, "The construction and evaluation of behavioral models for microwave devices based on time-domain large-signal measurements", *Proc. Int. Electron Devices Meeting*, pp. 819-822, 2000.
- [3] D. Root, J. Wood, A. Pekker, N. Tuffillaro and D. Schreurs, "Systematic behavioral modeling of nonlinear microwave/RF circuits in the time domain using techniques from nonlinear dynamical systems," *Proc. IEEE BMAS Workshop*, pp. 4.2.1-4.2-4, Santa Rosa, CA, Oct. 2002.
- [4] C. Borchers, "Symbolic behavioral model generation of nonlinear analog circuits," *IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 10, pp. 1362-1371, Oct. 1998.
- [5] J. Roychowdhury, "Reduced-order modeling of time-varying systems," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, pp. 1273-1288, 1999.
- [6] J. Roychowdhury, "Automated macromodeling of "nonlinear" wireless blocks," *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 2.4.1-2.4.4, 1999.
- [7] J. R. Phillips, "Projection-based approaches for reduction of weakly, nonlinear time-varying systems," *IEEE Trans. Computer-Aided Design*, vol. 22, pp. 171-187, Feb. 2003.
- [8] J. R. Phillips, "Automated extraction of nonlinear circuit macromodels," in *Proceedings Custom Integrated Circuit Conference*, pp. 451-454, May 2000.
- [9] X. Li, P. Li, Y. Xu and L. T. Pileggi, "Analog and RF circuit macromodels for system-level analysis," *Proceedings of Design Automation Conference (DAC)*, pp. 478-483, June 2-6, 2003.
- [10] H. A. Mantooth and P. E. Allen, "A higher level modeling procedure for analog integrated circuits," *J. Analog Integrated Circuits and Signal Processing*, vol. 3, pp. 181-195, May 1993.
- [11] V. Chaudhary, M. Francis, X. Huang, and H. A. Mantooth, "PARAGON - A mixed-signal behavioral modeling environment," *IEEE Intl. Conf. on Communications, Circuits, & Syst.*, pp. 1315-1321, China, June 30, 2002.
- [12] P. Mallick, M. Francis, V. Chandrasekhar, A. Austin and H. A. Mantooth, "Achieving language independence with Paragon," *IEEE Behavioral Modeling and Simulation Workshop (BMAS)*, pp. 149-153, San Jose, CA, Oct. 7-8, 2003.
- [13] X. Huang, C. Gathercole and H. A. Mantooth, "Modeling nonlinear dynamics in analog circuits via root localization", *IEEE Trans. Computer-Aided Design*, vol. 22, no. 7, pp. 895-907, July 2003.
- [14] P. J. Ashenden, G. D. Peterson, D. A. Teegarden, *The System Designer's Guide to VHDL-AMS*, Morgan-Kaufman, San Francisco, CA, 2003.
- [15] H. A. Mantooth and M. Fiegenbaum, *Modeling with an Analog Hardware Description Language*, Kluwer Academic Publishers, Norwell, MA, 1995.
- [16] R. S. Cooper, *The Designer's Guide to Analog and Mixed-Signal Modeling*, Avant! Press, 2001.