A Method for Parameter extraction of Analog Sine-wave Signals for Mixed-Signal Built-In-Self-Test Applications

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Abstract

This paper presents a method for extracting, in the digital domain, the main characteristic parameters of an analog sine-wave signal. The required circuitry for on-chip implementation is very simple and robust, which makes the present approach very suitable for BIST applications. Solutions in this sense are addressed together with simulation results that validate the feasibility of the proposed approach.

1. Introduction

Robust and efficient on-chip methods for the characterization of sine-wave signals is of undoubted interest. It comprises the measurement of parameters like frequency, amplitude, DC-level, distortion, signal-to-noise ratio, etc. It has a wide variety of potential applications in the field of analog and mixed-signal testing since most of these systems can be characterized by applying sinusoidal stimuli (filters, A/D and D/A converters, sigma-delta modulators, etc.). In addition, it is also a key point for the extension of the so-called Oscillation-Based-Test (OBT) [1, 2] to a full BIST scheme.

Traditionally frequency-related specifications are measured using periodic signals (square and/or sine-waves in the majority of cases) as test stimuli and applying complex processing algorithms (in the digital domain) to the response (DFT, FFT, etc.), in order to extract the targeted parameters. The direct emulation of this traditional method for on-chip implementation and BIST applications is not practical due to the excessive overhead, except in very complex systems where the required hardware is already available on-chip [3].

The use of ΣΔ-encoding schemes have been shown to be very efficient for on-chip signal generation and evaluation. In [4] the generation of precise single and multi-tone sine-waves is reported. On the other hand, the use of ΣΔ modulators as Analog Response Extractors has been proved to be useful [5]. The main advantages of these ΣΔ-based approaches are the simplicity and the robustness of the required circuitry, which make them very suitable for on-chip implementation, and hence, for BIST applications.

This work aims to improve and extend the capability of the ΣΔ scheme proposed in [6], for the extraction of the amplitude, frequency and DC-level of the input signal, including also the measurement of the harmonic distortion. A robust and area efficient signal analyzer for BIST applications is thus obtained. As the technique imposes certain requirements on the signals to be processed, a procedure for the efficient use and on-chip implementation is also addressed.

2. Review of the basic approach

Let be $x(t)$ a low distorted signal of period T, amplitude A and DC-level B. It can the be approximated by,

$$x(t) \approx B + A\sin(\omega t + \varphi) \qquad (1)$$

where $\omega = 2\pi/T$ and φ represents a phase-shift. A method for extracting the characteristic parameters of such signal was reported in [6]. The basis of the approach is based on the fact that,

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$$\frac{1}{T}\int_0^T x(t)dt = B$$
$$\frac{1}{T}\left[\int_0^{T/2} x(t)dt - \int_{T/2}^{T} x(t)dt\right] = \frac{2A}{\pi}\cos\varphi \quad (2)$$

Figure 1 illustrates the proposed implementation of the approach using a 1st-order ΣΔ modulator, a zero crossing detector and a set of simple digital counters. Signal $x(t)$ is fed into a zero-crossing detector and a 1st-order ΣΔ modulator. Notice that the generated square-wave signal SQ, that defines the integration intervals, is in phase with $x(t)$ so $\varphi \approx 0$ can be considered in (2).

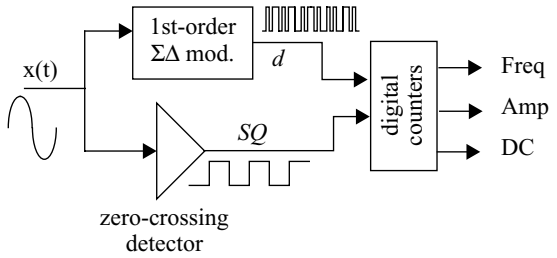

Figure 1:Block Diagram of the basic approach

The integration procedure is performed in the digital domain (using a set of counters) over the generated bit-stream d accordingly to the period of the square-wave SQ. In this way, it can be shown that a digitally encoded measurement of the signal frequency ($1/T$) referred to the sampling frequency ($1/T_s$), the amplitude referred to the modulator full-scale (A) and DC-level referred to the modulator full-scale (B) can be extracted at the end of each period of SQ as an integer number that can be expressed in the form [6],

$$Freq \approx (T/T_s) \pm 1$$
$$Amp \approx (2A/\pi)(T/T_s) \pm 2 \quad (3)$$
$$DC \approx B(T/T_s) \pm 1$$

The accuracy of the measurements is mainly determined by the oversampling ratio (T/T_s) and the quantization error, which introduces the bounded terms ($\pm 1, \pm 2$). The precision of the measurements can be improved by extending the measurement over a large number of periods and taking the mean value.

3. Improved and extended approach

The above approach requires that the square-wave be in phase with the main harmonic of the input signal and have a 50% duty-cycle. It restricts its application to low-distorted and low DC-level signals as the square wave is defined by the zero crossing points of the input signal. This section describes a way to overcome this problem.

Let us now consider that signal *x(t)* has harmonic components. It can be described in terms of its Fourier series expansion in the form:

$$x(t) = B + \sum_{k=1}^{4} A_k \sin(k\omega t + \phi_k) \quad (4)$$

where A_k represents the amplitude of the k-th harmonic component and ϕ_k its corresponding phase shift. For the sake of simplicity, we will restrict our discussion to the presence of a limited number of significant harmonics, namely 4. This is not an strong exigency as in many applications it uses to be the maximum number of harmonics of interest.

What was done in [6] was to multiply the modulator output bitstream by a square wave at the signal frequency. In this paper, the concept is similar but a modification is introduced as this multiplication is realized at the front-end of the modulator. As the phases ϕ_k of the harmonics are not *a priori* equal, two square waves in quadrature are needed to evaluate the power at a given frequency. Let be $SQ_k^T(t)$ a square wave of amplitude 1 and period *T/k* (the same as the signal k-th harmonic), and $SQ_k^{Td}(t)$ the square wave in quadrature with $SQ_k^T(t)$.

Figure 2 illustrates the block diagram of the modified approach. Signal *x(t)* is multiplied by the two square waves defined above. The resulting two signals are driven to two matched 1st-order ΣΔ-modulators. In a Switched-Capacitor realization, such multiplication can be performed inside the own modulator by a proper switching.

The response of a 1st-order modulator can be expressed in terms of the input signal '*y*' and the quantization error '*e*' as,

$$d(n) = y(n-1) + e(n) - e(n-1) \quad (5)$$

The sum of the bit-stream along a number '*q*' of samples is then given by,

$$\sum_{n=1}^{q} d(n) = \sum_{n=0}^{q-1} y(n) + \{e(q) - e(0)\} \quad (6)$$

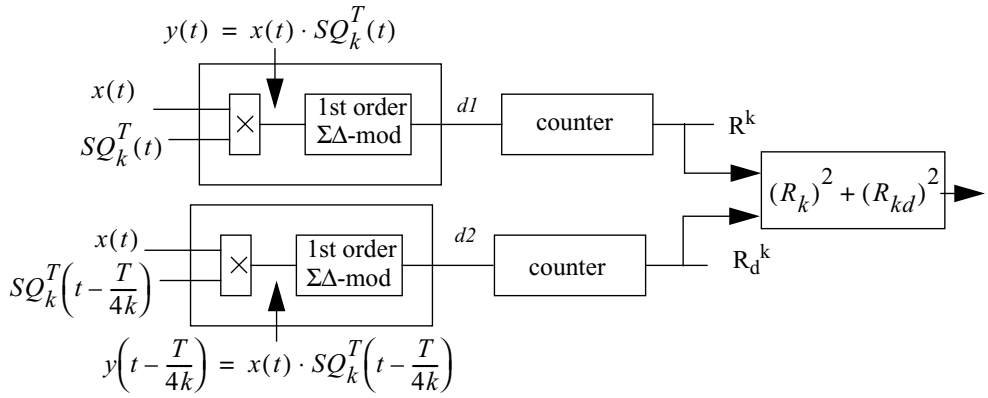

Figure 2:Modified scheme for the characterization of distorted sine-wave signals

Notice that, under the assumption of no over-range in the modulator ($e(n) \in [-1, 1]$), the integration of the bit-stream is equivalent to the discrete integration of the signal *y(n)* plus a term representing the quantization error limited to 2.

If the ratio of the sampling frequency to the input signal frequency $N=f_s/f=T/T_s$ in the modulator is high enough, the discrete summation of *y(n)* approaches to the continuous time integration of *y(t)*. So, if the sum is extended to an integer number of periods *M* of *x(t)* the result will be practically the same except for a quantization error term. In fact, it can be shown that the error due to sampling can be neglected with respect to the quantization error. In this way, the bit-streams at the output of each modulator are processed by simple digital counters as in [6]. The possibility to realize the measurement sequentially is discussed in Section 5. Two measures, R_k and R_{kd}, are thus obtained for the two square waves in quadrature $SQ_k^T(t)$ and $SQ_k^{Td}(t)$. Table I gives the expected counter values for each harmonic *k* as function of the oversampling ratio *N*, the number of averaging periods *M* and the input signal parameters (B,A_k and ϕ_k, k=1,2,3,4).

As $[(\sin x)^2+(\cos x)^2]=1$, it should be clear that each frequency component of *x(t)* can be estimated by computing $[(R_k)^2+(R_{kd})^2]$. Of course the measurement is affected by a bounded error, and hence, a result in terms of a confidence interval may be useful. For example, for *k*=2,3,4 it can be ensured that,

$$\left(\frac{2A_k}{\pi}\right)^2 \in \left(\frac{1}{MN}\right)^2 \begin{bmatrix} min\{(R_k+\varepsilon_k)^2 + (R_{kd}+\varepsilon_{kd})^2\} \\ max\{(R_k+\varepsilon_k)^2 + (R_{kd}+\varepsilon_{kd})^2\} \end{bmatrix} \quad (7)$$
$$|\varepsilon^k|, |\varepsilon_d^k| \in [-2, 2]$$

In the case of A_1, it appears with A_3 (*k=1*). However, if $A_1 \gg A_3$ as it is usual, the contribution of A_3 in *k=1* can be neglected (this is even more true if the summation is extended to a small number of periods). Otherwise, the contribution of A_3 can be subtracted as it is extracted when *k=3*.

Table I: Results at the output of the counters. (M=number of periods, N=Oversampling Ratio, $|\varepsilon|, |\varepsilon_d| \in [-2, 2]$

k	R_k	R_{kd}
0	$B(MN)+\varepsilon$	$B(MN)+\varepsilon_d$
1	$MN(2/\pi)[A_1\cos\varphi_1 + (A_3/3)\cos\varphi_3] + \varepsilon$	$MN(2/\pi)[A_1\sin\varphi_1 + (A_3/3)\sin\varphi_3] + \varepsilon_d$
2	$MN(2/\pi)[A_2\cos\varphi_2] + \varepsilon$	$MN(2/\pi)[A_2\sin\varphi_2] + \varepsilon_d$
3	$MN(2/\pi)[A_3\cos\varphi_3] + \varepsilon$	$MN(2/\pi)[A_3\sin\varphi_3] + \varepsilon_d$
4	$MN(2/\pi)[A_4\cos\varphi_4] + \varepsilon$	$MN(2/\pi)[A_4\sin\varphi_4] + \varepsilon_d$

4. Application example

The proposed approach has been emulated in SIMULINK/MATLAB. A realistic model for the ΣΔ modulator implemented using the guidelines reported in [7] has been used. The parameters which determine the modulator performance are shown in Table II.

Table II: ΣΔ modulator parameters. Values normalized with respect to a sampling period=1 when corresponds

GENERAL	Tsampling = 1 Full Scale Range= 1V
COMPARATOR	Hysteresis level = eps Input offset = 10mV
INTEGRATOR	Initial_state= random Saturation level= 3V Gain= 0.98
AMPLIFIER	Output_noise =1μV Slew_rate= 6 Gain_bandwidth=10/Tsampling dc_gain=80dB Feedback_capacitor=0.5pF Temperature= 300K

A signal containing three harmonics and a non zero DC level (Table III) has been used to validate the approach.

Table III: Signal components and values. Values (in dBms) are normalized with respect to the full-scale range of the modulator

Signal Components	Actual Value	
	(mV)	dBm
DC-level	8.9	-46.02
Main harmonic	910.0	-0.83
2nd harmonic	1.0	-60.0
3rd harmonic	0.1	-80.0

Figure 3 shows the confidence intervals obtained for an oversampling ratio (N) of 96 as a function of the number of periods (M) taken into account for evaluation. The results agree perfectly with the expected ones. That is, the larger the number of periods and the oversampling ratio, the larger the accuracy for a given magnitude.

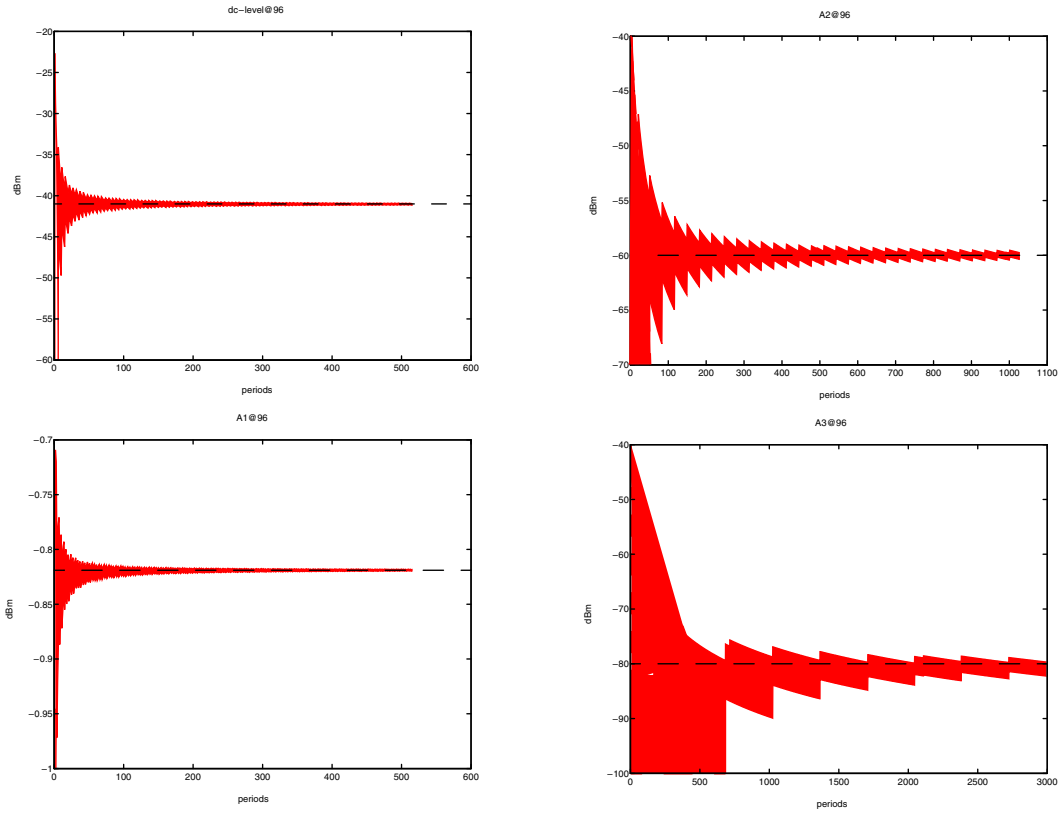

Figure 3:Confidence intervals versus number of periods taken for evaluation for an oversampling ratio of 96 obtained through Simulink/Matlab simulations

5. Practical considerations for BIST applications

As it was said in section 3, the work in [6] proposed to realize the multiplication by a square wave in the digital domain, at the output of the modulator. In principle, this could still be applied here, and all the R_k and R_{kd} measurements could be realized in parallel at the expense of one counter per parameter. However, the back-end multiplication leads to a loss of accuracy due to the incomplete cancellation of the quantization error in the modulator. For a same accuracy, the required number of samples would be much higher for the back-end than for the front-end multiplication. Hence, the measurement of small harmonics would require a prohibitive number of samples for the back-end modulation.

In a Switched-Capacitor realization, the front-end multiplication can be performed inside the own modulator by a proper switching. Nevertheless, a price has to be paid for this multiplication. The measurements can no longer be realized in parallel, unless more than one modulator is implemented. As can be seen in Figure 2, two matched modulators are used to calculate R_k and R_{kd} in parallel, in a way similar to an IQ demodulation scheme, but it would be possible to realize the measurements sequentially. Actually, a trade-off exists between test-time and area. If the measurements are realized sequentially, only one modulator and one counter are required plus some memory to store each R_k and R_{kd} value. If the measurements are realized fully in parallel, a modulator and a counter are required for each R_k or R_{kd}.

Another tricky point that has to be dealt with is the computation of the harmonic signatures $[(R_k)^2+(R_{kd})^2]$ that requires a squaring function. Notice that this function has only to be performed over a limited number of values (8 times for 4 harmonics), and can thus be realized sequentially in several clock cycles. Let us make a rough evaluation of the required resources for the case of sequential measurements, as shown in Figure 4. The counter output R_k is stored on an n-bit register. The value of n is determined by the wanted precision. The squaring function can be realized using a n-bit full-adder and a $2n$-bit register in n clock cycles. The result of this operation has to be stored for further processing, so another $2n$-bit register is needed. The squaring operation is repeated for R_{kd} with the same hardware. Then, the two squared values have to be summed so a $(2n)$-bit full-adder and a $(2n+1)$-bit register are needed. If the results for each harmonic are stored on chip, other 3 $(2n+1)$-bit registers are required. As a 2n-bit full-adder is used to do the final summation, the n-bit full-adder can be avoided. Therefore, the total hardware would consist of one $2n$-bit full adder, 4 $(2n+1)$-bit registers, 2 $2n$-bit registers and 2 n-bit registers (1 for the counter output and one to store the DC-level value that does not need any processing). A non-optimized implementation of a full-adder would require 28 transistors per bit and the registers would require 6 transistors per bit. Hence, this amounts to $140n+24$ transistors. The total computation time (for the 4 harmonics) can also be evaluated to about $8n+4$ clock cycles. Obviously, it is possible to optimize such hardware as the same precision may not be required for each harmonic.

Finally, the proposed method requires that the oversampling ratio of the modulator be an exact multiple of $\{4 \times max(k)\}$, where $max(k)$ refers to the maximum index of the harmonic to be isolated. Obviously, it needs to ensure that the sampling clock be synchronized with the signal to be evaluated.

A solution that accomplishes the cited requisite is illustrated in Figure 5-a. The required signals are generated by a digitizer and square-wave generators (shift registers) using the same Master Clock. In this way, synchronization is ensured. This solution is appropriate when the test signals are generated off-chip by an ATE. A more suitable solution for on-chip implementation consists on the use of the ΣΔ-encoded signal generator approach reported in [4] instead of a complete digitizer.

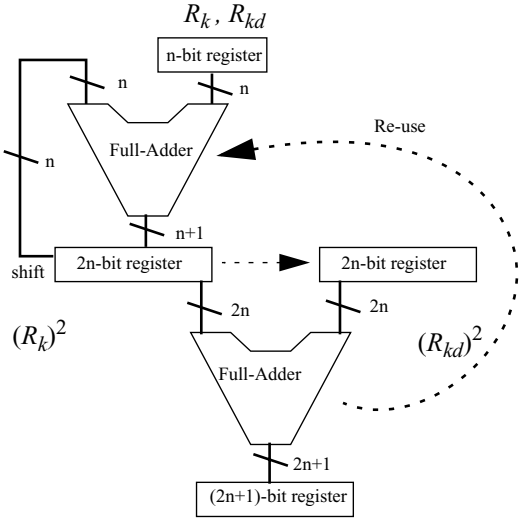

Figure 4:Possible implementation of the harmonic signature computation

However, the above solution limits the applicability of the approach to a reduced set of frequencies. Another solution that overcomes this problem is shown in Figure 5-b. The idea is to use a PLL to capture the frequency of the signal to be evaluated and generate a clock (of frequency multiple of $\{4 \times max(k)\}$) to be used as the clock for the parameter extractor circuit. The immediate future work will be focused on this line. That is, on the study and integration of a prototype for this solution.

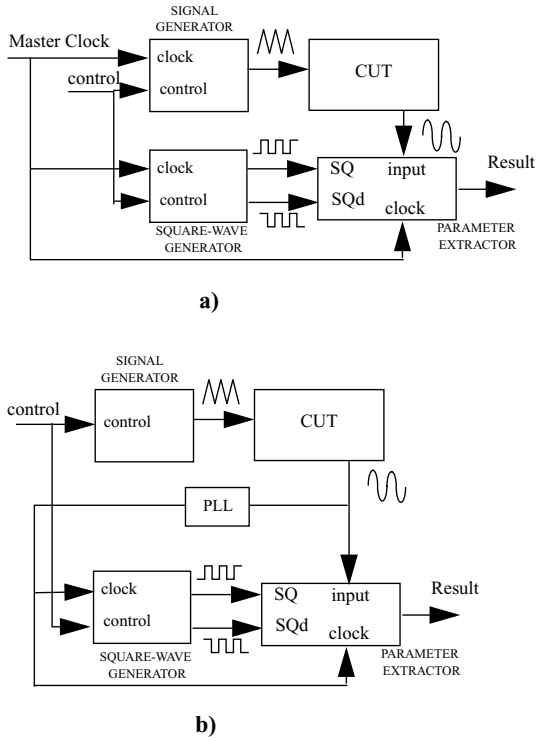

Figure 5:Integration of the proposed approach in a BIST scheme. a) Using an external Master Clock. b) Using a PLL

6. CONCLUSIONS

An approach for the characterization of sine-wave signals using first order ΣΔ modulators has been presented. It allows the estimation the DC-level and the amplitudes of the tones composing the signal. In first instance, the approach can be adapted to take into account a limited number of harmonics. The accuracy of the measurements is given by the relation between the input signal frequency and the sampling frequency of the modulator and the number of periods taken into account for the evaluation.

The required circuitry for the implementation of the approach is very simple and robust, a first order modulator and a simple digital logic, which makes the present approach very suitable for on-chip implementation. In addition, the main processing of the data are performed in the digital domain through basic arithmetic operations. Moreover, in a switched-capacitor realization of the scheme in Figure 2, the modulation of the input signal *x(t)* can be performed inside the modulator through a proper control of the switches and capacitors.

7. REFERENCES

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