A 2.7V 350µW 11-b Algorithmic Analog-to-Digital Converter with Single-Ended Multiplexed Inputs

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Abstract.

A low-power low-area CMOS algorithmic A/D converter that does not require trimming nor digital calibration is presented. The topology is based on a classical cyclic A/D conversion using a capacitor ratio-independent computation circuitry. All the nonidealities have been carefully analyzed and reduced by proper choices of design and layout solutions. As a result the errors coming from opamp offset and finite open-loop dc gain, switch charge injection and clock feedthrough, parasitic capacitors, and intrinsic noise sources are reduced under the LSB level. To process a multiplexed (8 channels) single-ended analog input, an efficient single-ended to fully differential circuit has been presented. The converter achieves 11 bit accuracy in the Nyquist band at a sampling rate of 8kSps. The total power dissipation is only 350µW at 2.7V supply voltage. The active area is 0.3 mm^2 in a 0.35µm 5 metal levels CMOS technology with double-poly linear capacitors.

1. Introduction

In today's System on Chip (SoC) the presence of the so-called "Auxiliary A/D Converter" (AuxADC) is often required. The aim of the mentioned converter is usually to perform several general-purpose measurements of both external and internal analog signals or to monitor some behaviors that require a time-driven feedback. Fig. 1 shows how the AuxADC could be inserted in a SoC. The required I/Os (apart the analog inputs and the Data outputs) are a voltage reference VREF, a bias current Ibias, an input clock signal Clk, a request signal to enable the conversion ADC_Req, and a power-down control signal PD. If the AuxADC is inserted in mobile equipment, such as a GSM cellular phone, the analog signals to be converted can be the battery voltage level, the voltage and current levels during battery charging, the quartz crystal oscillator and transmit power amplifier temperatures, some references, etc. Because these signals are low frequency or DC levels, the requirements for the AuxADC are low speed, moderate resolution (10 to 12 bits), multiplexing capability of several single-ended signals with different input range values, low power consumption, and low area occupancy. Multiplexing and low power requirements are key points in this case to increase the battery lifetime because this A/D converter is used all the time when the cellular phone is powered on, i.e. during both talk and stand-by times. Moreover, processing of single-ended inputs is very important as well because of the nature of the signals that are monitored. Finally, low silicon area is desired for cost reduction reasons.

In the literature there are several A/D converters fitting the above specifications, but unfortunately their architectures are somehow in conflict with the above-mentioned requirements. In fact, charge redistribution SAR A/D's require linear and matched capacitors leading to a large silicon area to implement 11-12 bit accuracy. Resistive arrays A/D topologies are limited to 9 bits by the resistance matching of today's technologies or require expensive trimming procedure. On the contrary, Sigma-Delta A/D's are very process insensitive, power and area efficient in short channel technologies, but cannot be used to process multiplexed input signal because there is no direct correspondence between an analog input sample and a digital output code.

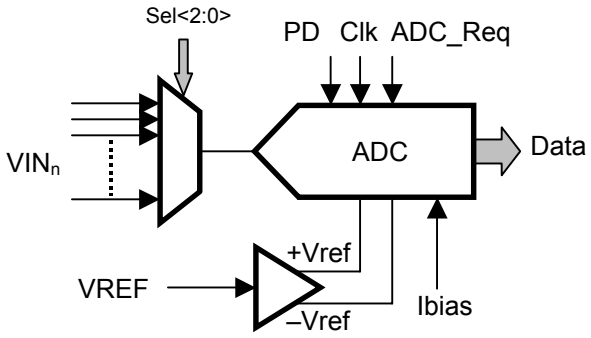

Fig. 1: Block diagram of the algorithmic A/D converter.

The cyclic or algorithmic A/D converters [1] could be a good compromise to satisfy the above requirements. This kind of converter doesn't needs matched capacitors, thus area and power consumption can potentially be very low (two opamps and one comparator). The main limitations of this architecture in reaching 12 bit resolutions are well known and resolved [1]. However, published solutions use high supply voltages (5V to 10V) that are advantageous for dynamic range but at the expense of higher power dissipation even at low speed [1-3] or use digital background calibration [4] that results into a huge area increase for the overall converter. Moreover, all these converters have fully differential inputs, while the kinds of signals to be monitored by a general purpose A/D converter are usually single-ended.

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In this paper a 2.7V low power low area algorithmic A/D converter that achieves 11 bit of accuracy at a sampling rate of 8kSps without requiring any additional calibration circuitry is presented. It also performs a single-ended to fully differential conversion on 8 multiplexed analog input signals (channels) without any penalty in area and consumption.

In Section 2 the principle and description of the algorithmic A/D converter is reviewed, and two methods to perform single-ended to fully differential conversion of the input signal are considered and analyzed. In Section 3 the limiting factors to reach 11-b accuracy are presented, while some experimental results are reported in Section 4.

2. Circuit Description

The algorithmic A/D converter schematic is illustrated in Fig. 2, where its equivalent single-ended version is shown for simplicity. It consists of an analog signal loop which contains a Sample&Hold amplifier (SHA), a comparator (COMP), a multiply-by-two amplifier, and a reference subtraction circuit. The last two functions are performed together with the same amplifier (MULT_SUBT). The operation of the converter consists of first sampling the input single-ended signal onto the SHA while converting it into a fully differential form, as will be shown later. After that, the input switch is disconnected and a conventional restoring cyclic conversion algorithm begins. The implementation of the multiply-by-two amplifier is ratio-independent to avoid the well known errors due to capacitor mismatch. The SHA output is sampled on C_2 in the first clock cycle, then transferred onto feedback capacitor C_3 during the second clock cycle while subtracting at the same time $\pm V_{ref}$ according to the (n-1) bit state. Subsequently, during the third clock cycle, the top plate of C_3 is disconnected from the opamp feedback and the SHA output is re-sampled on C_2. During the fourth clock cycle C_2 is put in the opamp feedback while C_3 charge is redistributed back onto the capacitor C_2, and the OPA2 output voltage is sampled on C_1 of the SHA. The operation takes four clock cycles per 1-bit conversion, therefore a 12-b conversion

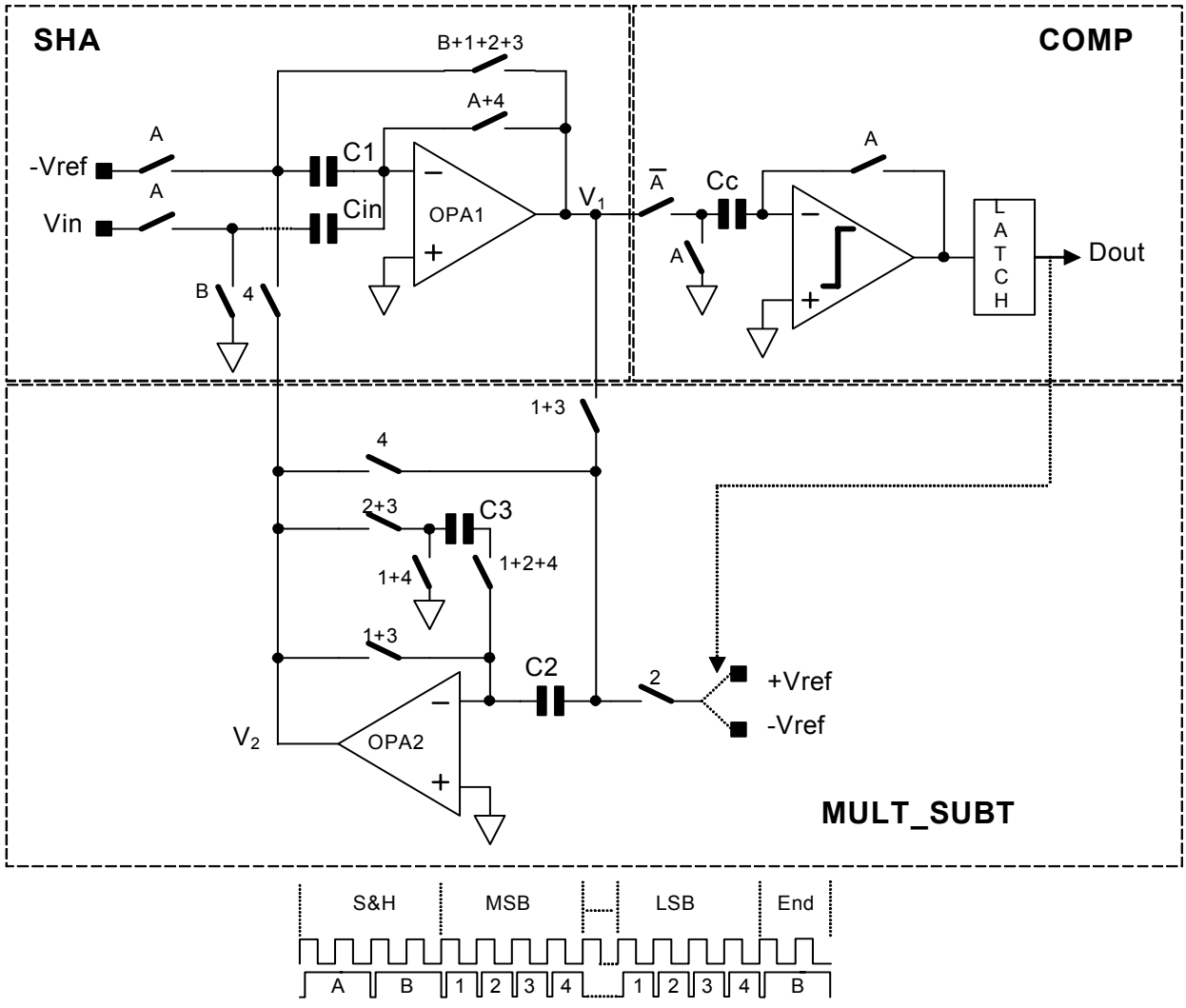

Fig. 2: A/D converter schematic and switching timing.

takes (12×4 + 4 + 2) = 54 clock cycles, where additional 4 cycles are needed for the input sampling and switching initialization, and 2 cycles are used for reset purpose before the next conversion. Notice that, with a target accuracy of 11 bits, a 12-bit resolution has been chosen to reduce the converter quantization noise and leave some more room to the other noise sources as kT/C, thermal, and flicker. An internal differential reference generator and a common-mode voltage (V_{cm}) circuit have been derived from the VREF input pin.

Single-Ended to Fully-differential Conversion

The single-ended to fully differential conversion is implemented in the SHA, as shown in Fig. 3.

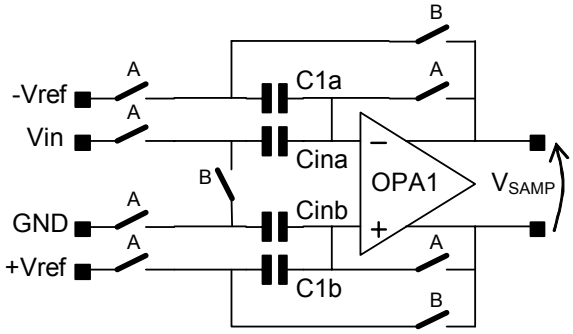

Fig. 3: Single-ended to fully-differential SHA.

During phase A, V_{in} is sampled by C_{ina}, C_{inb} is tied to ground, and $-V_{ref}$ and $+V_{ref}$ are stored onto C_{1a} and C_{1b} respectively. During phase B, C_{1a} and C_{1b} are put in the opamp feedback, while the bottom plates of C_{ina} and C_{inb} are connected together and left floating performing the single-ended to differential conversion on the SHA output, resulting:

$$V_{samp} = -2V_{ref} + \left(\frac{C_{in}}{C_1}\right)V_{in} \qquad (1)$$

Changing in (1) the value of C_{in} according to the selected input channel, any input voltage range from ground to the supply (or even higher than the supply) can be converted into a fully differential signal from $-2V_{ref}$ to $+2V_{ref}$.

As soon as the input sampling phase is completed, the top plates of C_{ina} and C_{inb} are disconnected from the opamp inputs (switches not shown in Fig.3), thus maximizing the opamp loop gain during the following bit conversion cycles. A big advantage of the floating input sampling structure is that the common-mode of the input signal is not transmitted to the opamp inputs; therefore there is no need for high Common-Mode Rejection Ratio (CMRR) or large input voltage capability for the opamp input stage. This can be better understood by comparing the behaviors during the hold phase of the two SHA's with grounded and floating input sampling capacitors shown in Fig. 4a and 4b, respectively. Assuming that the opamp common-mode output voltage is forced to V_{cm} by the common-mode feedback circuit and $V_x^+ = V_x^-$ for the virtual ground principle, it can be easily demonstrated that the opamp common mode input voltage V_x is given by:

$$V_X = \frac{5V_{cm} - V_{in}}{3} \quad \text{for the grounded sampling capacitor}$$

$$V_X = V_{cm} \quad \text{for the floating sampling capacitor}$$

and the voltage V_{fl} on the floating node in Fig. 4b is:

$$V_{fl} = \frac{V_{in}}{2}$$

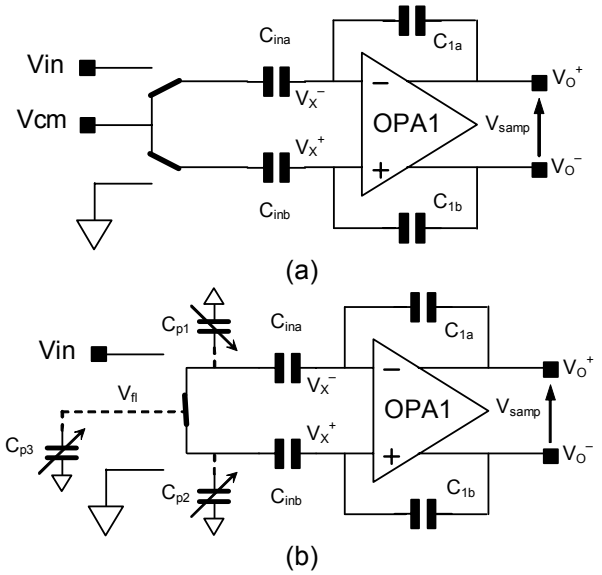

Fig. 4: SHA with a) grounded and b) floating input sampling capacitors.

The presence of non-linear parasitic capacitances at the floating node, i.e. the channel capacitance C_{p3} of the CMOS switch shorting the input capacitors bottom plates and the capacitances C_{p1} and C_{p2} of the source/drain diffusions connected to the bottom plates, can potentially be a drawback for this structure. In fact, these non-linear capacitances must be (dis-)charged to $V_{in}/2$ by a current that flows from the opamp output through the feedback and input capacitors, resulting into harmonic distortion on the SHA output if the upper and lower paths of the fully differential circuit are not matched. It can be demonstrated that, in presence of a mismatch ΔC_1 between C_{1a} and C_{1b}, the relationship between V_{samp} and Vin is given by

$$\frac{V_{samp}}{V_{in}} \cong 1 + \frac{\Delta C_1}{C_1} \cdot \frac{C_{p3} + C_{p2} - C_{p1}}{8C_1} \qquad (2)$$

However, because the parasitic capacitances are much lower than C_1, simulations have showed that the total harmonic distortion can be kept well under –90dB even in

the case of mismatches as high as 1% (at 5σ). A similar result applies for a mismatch between C_{ina} and C_{inb}.

3. Converter Nonidealities

Even if the loop operation is based on a capacitor mismatch-independent structure, opamp offset and finite open-loop dc gain, switch charge injection and clock feedthrough, and parasitic capacitor deteriorate the accuracy of the ideal multiplication-by-two in the loop.

The offset voltage effect is reduced by a classical autozero method in the two opamps and comparator during the input sampling phase and every bit conversion cycle. High opamp open-loop dc gain is needed to ensure complete charge transfer into the feedback capacitors.

It can be demonstrated that:

$$V_1(i+1) = \frac{2V_1(i)\left(1-\frac{1}{2A_2}\right) - Vref \cdot b(i)\left(1-\frac{1}{A_2}\right) + V_{off2}\frac{3}{A_2}}{\left(1+\frac{2}{A_2}\right)\left(1+\frac{1}{A_1}\right)} + \frac{V_{off1}}{A_1\left(1+\frac{1}{A_1}\right)} \quad (3)$$

with b(i) = 1 if $V_1(i) > 0$ or b(i) = -1 if $V_1(i) < 0$, and $V_1(1) = V_{samp}$.

A_1 (A_2) and V_{off1} (V_{off2}) are the open-loop dc gain and input-referred offset voltage of OPA1 (OPA2), respectively. By iterating this expression, for a 12 bit resolution a minimum open-loop dc gain of 80dB is required in the proposed converter architecture. To reach this gain requirement at 2.7V, a two-stage CMOS OTA with cascode compensation has been designed with 0.01% settling time capability within a clock cycle. The OTA schematic is shown in Fig. 5.

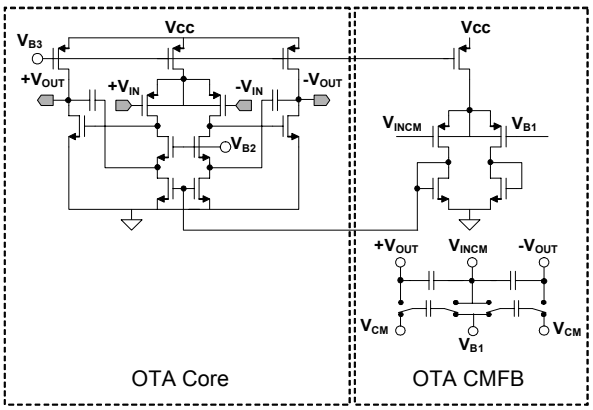

Fig. 5: OTA schematic.

Non-linear charge injection and clock feedthrough effects from MOS switches are reduced by using a classical four phase switching scheme [5], [6] and a fully-differential structure, while any residual charge effect or feedthrough due to mismatches in the two halves of the fully-differential path is minimized by using minimum switches close each other. With unit capacitors of 2pF, worst-cases simulations show that the effects of these nonidealities can be kept well below ½ LSB at 11-bit level. This unit capacitor value, which is quite small if compared to the previous art, has been chosen to limit the area and power consumption of the converter as much as possible. However, with such a low value a second order limiting effect becomes really important for resolution of 10b or more. In fact, the parasitic capacitances between the inputs and the outputs of each opamps introduce gain errors on both the SHA and the multiply-by-two amplifier according to the following formulas:

$$V_1(i+1) = V_2(i)\left(1-\frac{C_{PAR1}}{C_1}\right) \quad (4)$$

$$V_2(i+1) = \left(1-\frac{C_{PAR2}}{C_2}\right)\cdot \left[2V_1(i+1)\left(1-\frac{C_{PAR2}}{2C_3}\right) - Vref \cdot b(i)\left(1-\frac{C_{PAR2}}{C_3}\right)\right]$$

where C_{par1} and C_{par2} are the parasitic capacitances between input and output of OPA1 and OPA2, respectively. In a previous version of the same A/D converter prototype it has been experienced that few tens of μm of parallel tracks could lead to more than 1fF of parasitic capacitor, resulting into an error of 0.05% in the above formulas, therefore limiting the available accuracy to 10 bits.

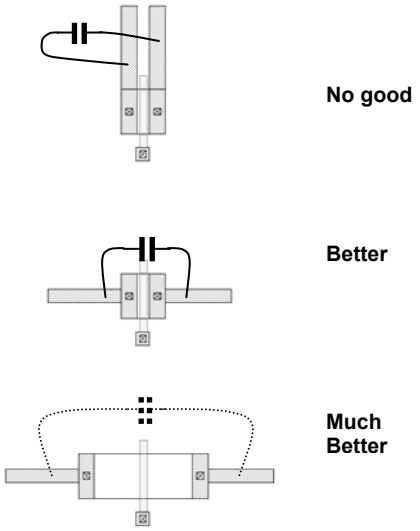

Fig. 6: Possible solutions for the layout of the reset switches.

To reduce this effect as much as possible, special care has been taken in routing the opamps inputs and outputs and proper ground shields have been inserted to avoid lateral and cross coupling between these nodes. Moreover, special

attention has been paid for the layout of the reset switches in the opamp feedback, as shown in Fig. 6.

4. Experimental Results

The presented experimental data and performance were achieved by setting Cin = 2C1, resulting into an analog input voltage range of 0÷2V, and with a sampling frequency of 8kSps. The prototype microphotograph is shown in Fig. 7. Active area is 0.3mm^2 in a 0.35µm 5 metal levels CMOS technology with double-poly linear capacitors. No effort has been made to match the capacitors using process insensitive geometries, such as dummy structures or top-plate corner rounding. The total power dissipation is only 350µW at 2.7V supply voltage including internal differential reference and common-mode voltage generators. The dynamic behavior of the converter has been tested in two ways, i.e. first using the code density test [7], and then performing a Fast Fourier Transform of the output. Plots of DNL and INL errors versus code of a typical sample are shown in Figg. 8a and 8b, respectively. Figg. 9a and 9b illustrate the output spectrum of the converter with a full-scale input signal of 200Hz and 3.4kHz, respectively. Finally, Fig. 10 shows the Signal-to-Noise and Distortion Ratio (SINAD) versus input level (1kHz input signal frequency). A dynamic range of 68dB, i.e. 11 bit accuracy, over the Nyquist band has been achieved. Table I summarizes the overall performance of the algorithmic A/D converter.

Using the classical ADC figure of merit $F = 2^{SNRbits} \cdot f_{SAMP} / P_{diss}$ reported in [8], this converter performs $F = 5.0 \cdot 10^{10}$ which is better or much better than previous similar algorithmic solutions [1-4], but it's close to the mean if other kinds of ADC architectures are considered. However, another facet of ADC performance is silicon area A. Generally the highest performance converters also have the most area. A convenient way to include A in the performance comparison is to use a modified figure of merit: $F_A = 2^{SNRbits} \cdot f_{SAMP} / P_{diss} \cdot A$. This converter presents $F_A = 1.7 \cdot 10^{17}$ which is near the top with respect to the published ADC solutions.

5. Conclusions

The design and implementation of a low-power low-area 11-b CMOS algorithmic A/D converter able to process multiplexed single-ended analog input signal have been presented. An efficient single-ended to fully differential conversion circuit has been considered and its advantage and drawback analyzed. Most of the non-idealities of the conversion loop have been reviewed and a new one has been reported. This type of A/D converter can be integrated as auxiliary measurement block inside a SoC where small area and very low power dissipation are of paramount importance.

6. Aknowledgements

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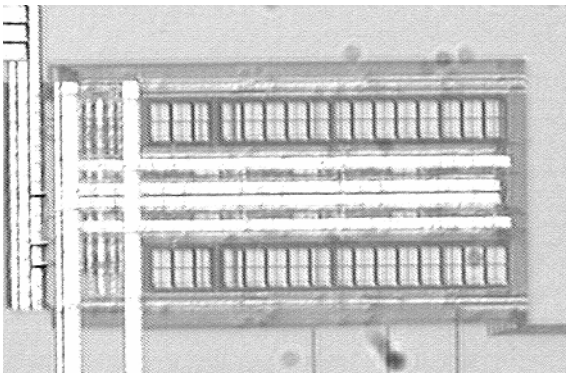

Fig. 7: Prototype microphotograph.

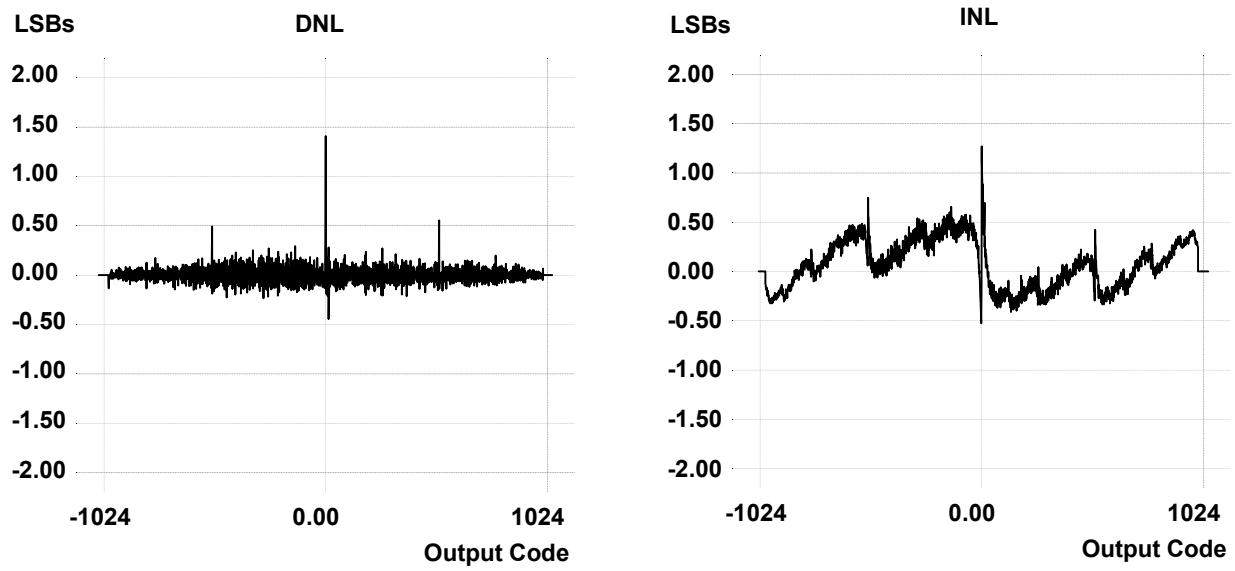

Fig. 8: a) DNL and b) INL versus output code.

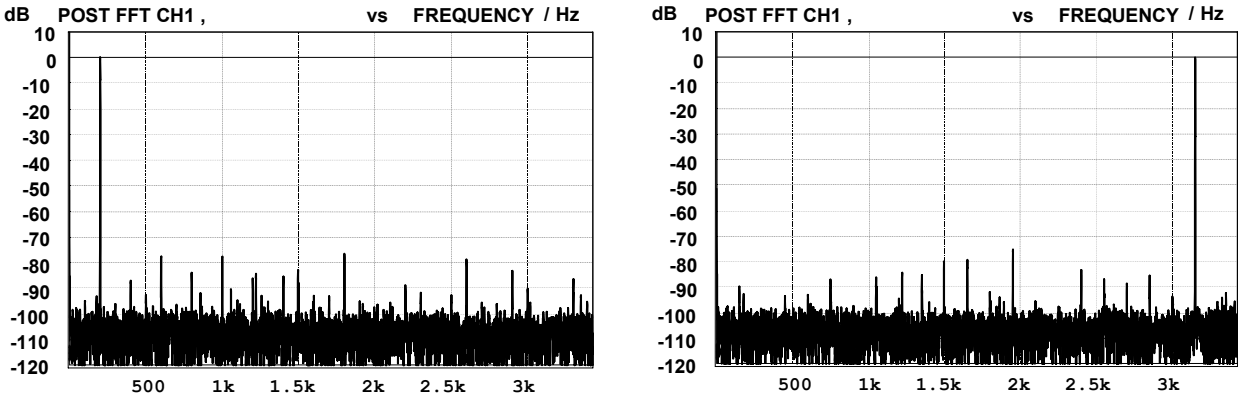

Fig. 9: Output spectrum with a) f_{IN} = 200Hz and b) f_{IN} = 3.4kHz.

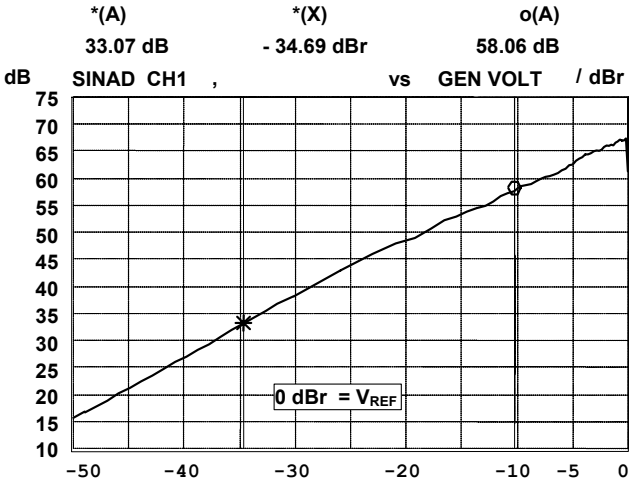

Fig. 10: SINAD versus input level (f_{IN} = 1kHz)

Table I - Performance summary

Nr. of input channels	8
Resolution	12 bits
Conversion rate (f_{CONV})	8 kSps
Input clock frequency	54 * f_{CONV}
DNL	+1.4 / –0.5 LSB
INL	+1.4 / –0.5 LSB
SINAD (peak)	67.8 dB
Dynamic Range	68 dB
THD	–72 dB
SFDR	75 dB
PSRR	50 dB
Gain error	0.1 dB
Offset error	2 LSB
Power supply	2.7 V
Current Consumption	130 µA
Active Area	0.3 mm^2