

Level of Similarity: A Metric for Fault Collapsing

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Abstract

We describe a new approach to fault collapsing that extends fault collapsing based on fault equivalence and fault dominance. The new approach is based on a metric called level of similarity between faults. Informally, a fault f_j is said to be similar to a fault f_i with a level of similarity $SL_{i,j} \leq 1$ if a fraction $SL_{i,j}$ of the tests for f_i also detect f_j . If $SL_{i,j}$ is high enough, one may exclude f_j from the set of target faults and rely on the test for f_i (and tests for other faults) to detect f_j . We describe a procedure for fault collapsing based on the level of similarity, and study its effectiveness experimentally.

1. Introduction

The concepts of fault equivalence and fault dominance are used in test generation to reduce the number of faults targeted. This is referred to as fault collapsing [1]-[4]. If two faults are equivalent, only one of them needs to be considered during test generation. As soon as one fault is detected, the other one is guaranteed to be detected as well. Similarly, if a fault f_j dominates a fault f_i and f_i is detectable, only f_i needs to be considered during test generation. As soon as f_i is detected, f_j is guaranteed to be detected as well.

In circuits with very large numbers of faults, fault collapsing beyond that based on fault equivalence or fault dominance may be needed for producing a set of target faults of reasonable size. Fault sampling can be used in this case to reduce the size of the set of target faults [5]-[7]. However, unlike fault collapsing, fault sampling cannot provide a single set of faults whose detection guarantees the detection of all the detectable circuit faults.

In order to improve the ability of fault collapsing to reduce the set of target faults, we extend the concepts of fault equivalence and fault dominance into the *level of similarity* between faults. Informally, a fault f_j is said to be similar to a fault f_i with a level of similarity $SL_{i,j} \leq 1$ if a fraction $SL_{i,j}$ of the tests for f_i also detect f_j . In this case, a test for f_i will detect f_j with probability $SL_{i,j}$. If $SL_{i,j}$ is high enough, one may exclude f_j from the set of target faults and rely on the test for f_i to detect f_j as well. If the set of target faults includes, in addition to f_i , also

faults $f_{i1}, f_{i2}, \dots, f_{im}$ such that $SL_{i1,j}, SL_{i2,j}, \dots, SL_{im,j} > 0$, the probability of detecting f_j without targeting it explicitly is even higher.

We define the level of similarity in Section 2. We discuss ways of computing it in Section 3. We then describe a procedure for fault collapsing based on the level of similarity in Section 4. We study the effectiveness of fault collapsing based on the level of similarity experimentally in Section 5. Specifically, we identify a minimum level of similarity that will allow us to perform fault collapsing without losing fault coverage in benchmark circuits.

2. The level of similarity

We use the following definition of equivalence, which is different from functional equivalence [2] for circuits with multiple outputs. This definition is useful when equivalence is used to perform fault collapsing.

Definition 1: Faults f_i and f_j are said to be equivalent if the set of input vectors T_i that detect f_i and the set of input vectors T_j that detect f_j are identical. Here, T_i and T_j are formed out of the set of all the possible input vectors of the circuit.

We use the following definition of fault dominance.

Definition 2: Fault f_j is said to dominate fault f_i if the set of input vectors T_i that detect f_i and the set of input vectors T_j that detect f_j satisfy the condition $T_i \subseteq T_j$.

We extend these definitions into a definition of the level of similarity between faults as follows. Equivalent faults have identical sets of input vectors that detect them, and we would like their level of similarity to be one. For non-equivalent faults, we would like the level of similarity to reflect the amount of overlap between the sets of input vectors that detect them. We use the following definition.

Definition 3: Let T_i be the set of input vectors that detect a fault f_i and let T_j be the set of input vectors that detect a fault f_j . Let f_i and f_j be detectable faults, i.e., $T_i \neq \emptyset$ and $T_j \neq \emptyset$. The level of similarity of f_j relative to f_i is $SL_{i,j} = |T_i \cap T_j| / |T_i|$.

It is important to note that the level of similarity is not symmetric, i.e., we can have $SL_{i,j} \neq SL_{j,i}$. We demonstrate this point below.

The following special cases are of interest. If f_i and f_j are equivalent, i.e., $T_i = T_j$, we obtain $T_i \cap T_j = T_i = T_j$, and $SL_{i,j} = SL_{j,i} = 1$. If f_j dominates f_i , i.e., $T_i \subseteq T_j$, we obtain $T_i \cap T_j = T_i$ and $SL_{i,j} = 1$. For $SL_{j,i}$ we obtain in this case $SL_{j,i} = |T_i| / |T_j| < 1$. In

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all other cases as well we obtain $SL_{i,j}, SL_{j,i} < 1$.

The level of similarity $SL_{i,j}$ has the following meaning. Suppose that a test set T includes a test $t \in T_i$ for a fault f_i . The probability that t is also a test for f_j is equal to the probability that $t \in T_j$, or $t \in T_i \cap T_j$. This probability is equal to $|T_i \cap T_j|/|T_i|$, which is the level of similarity $SL_{i,j}$. Thus, the level of similarity $SL_{i,j}$ is also the probability that a test for f_i will detect f_j . The higher the level of similarity $SL_{i,j}$, the more likely it is that a test for f_i will also detect f_j . For equivalent faults and when f_j dominates f_i this probability is 1.

We provide several examples of the level of similarity next. We use the combinational logic of MCNC finite-state machine benchmark *lion* for this example. The circuit has four inputs, 16 input vectors, and 40 faults, f_0, \dots, f_{39} . We represent an input vector by its decimal value. Thus, the input vectors are 0,1, \dots , 15. As before, we denote by T_i the set of input vectors that detect f_i .

For f_0 we have $T_0 = \{9, 10, 11, 12, 13, 14, 15\}$ and for f_2 we have $T_2 = \{4, 7, 13\}$. We have $T_0 \cap T_2 = \{13\}$. Therefore, $SL_{0,2} = 1/7 = 0.14$ and $SL_{2,0} = 1/3 = 0.33$.

For f_4 we have $T_4 = \{2, 6, 7, 10, 14, 15\}$. We have $T_0 \cap T_4 = \{10, 14, 15\}$. Therefore, $SL_{0,4} = 3/7 = 0.42$ and $SL_{4,0} = 3/6 = 0.5$.

For f_3 we have $T_3 = \{0, 3, 9\}$ and for f_{10} we have $T_{10} = \{0\}$. We have $T_{10} \subset T_3$ and $T_3 \cap T_{10} = T_{10} = \{0\}$. In this case, $SL_{3,10} = 1/3 = 0.33$ and $SL_{10,3} = 1/1 = 1$.

3. Computing the level of similarity

Computation of the level of similarity can be done in one of several ways, discussed next.

For circuits with small numbers of inputs it is possible to enumerate all the input vectors, find the sets T_i explicitly, and use set operations to compute the exact level of similarity as in the example above. We use this approach for circuits with small numbers of inputs.

For circuits with large numbers of inputs it is possible to use the same procedure as above but with a set of random vectors of limited size. The random vectors will allow us to find approximate values of $SL_{i,j}$, which are expected to be accurate enough for fault collapsing using the proposed concept of level of similarity. This is one of the approaches we use in this work for circuits with large numbers of inputs.

Another procedure for computing the level of similarity is described next. The procedure uses a partition of the circuit into fanout free regions to compute levels of similarity between faults in the same fanout free region. We use this procedure in this work as an alternative to the use of a set of input vectors. We use it for circuits with small as well as large numbers of inputs.

A fanout free region is a single-output subcircuit that has the following properties. (1) Its output is either a fanout stem or a primary output. (2) Its inputs are either fanout branches or primary inputs. (3) It does not include any fanout stems except possibly its output. We compute $SL_{i,j}$ for faults f_i, f_j only if f_i and f_j are contained in the

same fanout free region R . Furthermore, we require that the number of inputs to R would not exceed a constant denoted by N_R . Otherwise, we set $SL_{i,j} = 0$. The implication of setting $SL_{i,j} = 0$ to fault collapsing is that f_i will not be used for removing f_j from the set of target faults. The advantage of using fanout free regions is that the level of similarity can be computed efficiently.

We compute $SL_{i,j}$ for f_i, f_j in a fanout free region R with at most N_R inputs by considering R as if it were the complete circuit, and applying Definition 3 to the set of input vectors of R . Let the set of inputs of R be I . Initially, $T_i = T_j = \emptyset$. We consider the $2^{|I|}$ input vectors of R one at a time. For every input vector v , we apply v to R and simulate f_i and f_j in R . If v detects f_i (f_j) on the output of R (i.e., v propagates a fault effect to the output of R), we add v to T_i (T_j). At the end of this process, T_i (T_j) includes all the input vectors of R that detect f_i (f_j) on the output of R . We define $SL_{i,j}$ using T_i and T_j as in Definition 3, i.e., we set $SL_{i,j} = |T_i \cap T_j|/|T_i|$.

It is also possible to consider fanout free regions with larger numbers of inputs by using a limited number of random vectors for such regions.

Inaccuracies in the computation of $SL_{i,j}$ using fanout free regions can result from the following. (1) An input vector v of R may not be justifiable in the complete circuit. Thus, its contribution should not be counted in an accurate computation of $SL_{i,j}$. (2) A fault effect produced on the output of R by a vector v may not be propagatable to a primary output. In this case also, the contribution of v should not be counted in an accurate computation of $SL_{i,j}$.

4. Application to fault collapsing

Fault collapsing based on fault equivalence reduces the set of faults that need to be targeted during test generation by removing a fault f_j from the set of target faults if it is known to be equivalent to a fault f_i , which is included in the set of target faults. Fault collapsing based on fault dominance removes a fault f_j from the set of target faults if it is known that f_j dominates a fault f_i , which is included in the set of target faults. In this section, we extend the ability to reduce the set of target faults by performing fault collapsing based on the level of similarity.

Fault equivalence and fault dominance are binary properties, i.e., a pair of faults either have an equivalence (dominance) relation or not. The level of similarity has a continuum of values. Therefore, to perform fault collapsing based on the level of similarity, it is necessary to define a constant level of similarity above which a fault would be considered similar enough to another fault to be excluded from the set of target faults. We denote this constant by SL_{MIN} . If $SL_{i,j} \geq SL_{MIN}$, fault collapsing based on the level of similarity can exclude f_j from the set of target faults and keep only f_i .

By varying SL_{MIN} , we study the extent to which fault collapsing based on the level of similarity can reduce the set of target faults while still ensuring that all the detectable faults would be detected by a test set generated

for the collapsed set of faults. To facilitate the consideration of different levels of similarity, we truncate the similarity level $SL_{i,j}$ to two digits after the decimal point for every pair of faults f_i, f_j . Thus, $SL_{i,j}, SL_{MIN} \in \{0, 0.01, 0.02, \dots, 1\}$.

For a given SL_{MIN} , we perform fault collapsing based on the level of similarity as follows. Initially, all the circuit faults are included in the set of target faults CF , and all the faults are unmarked. We remove faults from CF as follows. For every $f_i, f_j \in CF$, if $SL_{i,j} \geq SL_{MIN}$ and f_j is unmarked, we remove f_j from CF and we mark f_i . The marking of f_i indicates that a fault was removed from CF because it is similar to f_i . This dictates that f_i needs to be kept in CF for the reason demonstrated next.

Consider three faults f_0, f_1, f_2 with sets of input vectors that detect them $T_0 = \{0,1,2,3,4\}$, $T_1 = \{3,4,5\}$ and $T_2 = \{5,6\}$. Let $SL_{MIN} = 0.5$. There are two fault pairs with $SL_{i,j} \geq 0.5$, f_1, f_0 with $SL_{1,0} = 0.66$ and f_2, f_1 with $SL_{2,1} = 0.5$. Suppose that we first eliminate f_0 from CF due to f_1 , and then eliminate f_1 from CF due to f_2 . The implication is that a test for f_2 needs to detect f_1 , which in turn needs to lead to the detection of f_0 . However, $SL_{2,0} = 0$ since none of the tests for f_2 detects f_0 . By marking f_1 after f_0 is removed from CF , we ensure that f_1 will not be removed due to f_2 .

The procedure for fault collapsing based on the level of similarity is given next.

Procedure 1: Fault collapsing based on the level of similarity with level SL_{MIN}

- (1) Let CF include all the target faults. For every $f_i, f_j \in CF$ compute the level of similarity $SL_{i,j}$ and truncate it to two digits after the decimal point. Unmark all the faults in CF .
- (2) For every $f_i, f_j \in CF$, if $SL_{i,j} \geq SL_{MIN}$ and f_j is unmarked, remove f_j from CF and mark f_i .

We demonstrate Procedure 1 by considering 12 of the faults of ISCAS-85 benchmark circuit *c 17* (the faults were selected for illustration purposes). The values of $SL_{i,j}$ for this circuit are shown in Table 1. These values were computed by applying Definition 3 to the set of all the input vectors of the circuit and considering only cases where $i \neq j$. We apply Procedure 1 using $SL_{MIN} = 0.20$. The fault pairs considered by Procedure 1 are the following.

Table 1: Levels of similarity for *c 17*

	0	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0.16	0.16	0	0.33	0.33	0	0	0	0.16
1	0	0	0.25	0	0.50	0	0	0	0	0	0	0.50
2	0	0.16	0	0	0	0	0	0	0.66	0.66	0.33	0.33
3	0.16	0	0	0	0	0.16	0	0	0.50	0.33	0.33	0.33
4	0.16	0.33	0	0	0	0.16	0	0	0	0	0	0
5	0	0	0	0.16	0.16	0	0.33	0.33	0	0	0	0.16
6	0.50	0	0	0	0	0.50	0	0.50	0	0	0	0
7	0.50	0	0	0	0	0.50	0.50	0	0	0	0	0
8	0	0	0.36	0.27	0	0	0	0	0	0.90	0.54	0
9	0	0	0.40	0.20	0	0	0	0	1.00	0	0.50	0
10	0	0	0.33	0.33	0	0	0	0	1.00	0.83	0	0
11	0.16	0.33	0.33	0.33	0	0.16	0	0	0	0	0	0

The faults f_0, f_6 with $SL_{0,6} = 0.33 \geq 0.20$. We remove f_6 from CF and we mark f_0 .

The faults f_0, f_7 with $SL_{0,7} = 0.33 \geq 0.20$. We remove f_7 from CF (f_0 is already marked).

The faults f_1, f_2 followed by f_1, f_4 and f_1, f_{11} . We remove f_2 from CF and we mark f_1 . We then remove f_4 and f_{11} from CF .

The pairs $f_{2,j}$ for $j = 8, 9, 10, 11$ are not considered since f_2 (and f_{11}) have already been removed.

The faults f_3, f_8 followed by f_3, f_9 and f_3, f_{10} . We remove f_8 from CF and we mark f_3 . We then remove f_9 and f_{10} from CF .

The faults that remain in CF are f_0, f_1, f_3 and f_5 . Considering f_4 that was removed from CF , we have $SL_{0,4} = 0.16$, $SL_{1,4} = 0.50$, $SL_{3,4} = 0$ and $SL_{5,4} = 0.16$. Thus, three faults in CF can contribute to the detection of f_4 . The probability that f_4 will be detected by a test set generated for CF can be approximated as $1 - (1 - 0.16)(1 - 0.50)(1 - 0.16) = 0.65$. This is higher than SL_{MIN} , and higher than $SL_{1,4} = 0.50$ because of which f_4 was removed from CF . For f_{11} , the probability that it will be detected by a test set for CF is approximately $1 - (1 - 0.16)(1 - 0.50)(1 - 0.33)(1 - 0.16) = 0.76$.

5. Experimental results

In the following subsections we describe a test generation procedure that will allow us to evaluate the effectiveness of fault collapsing based on the level of similarity. We then present experimental results.

The test generation procedure we use is based on test selection. This approach has the advantage that it always selects the same test when given the same fault, independent of other faults that need to be targeted.

For every circuit considered we use a set of input vectors U to perform test selection. When the level of similarity is computed based on a set of input vectors, we use the same set U for this purpose as well. For circuits with small numbers of inputs, U is the set of all the input vectors. For circuits with large numbers of inputs (larger than 14), U is a set of 20,000 random vectors.

We denote by F the set of all the circuit faults after they have been collapsed using the conventional approach, where fault collapsing is done using equivalence relations among faults on the inputs and output of the same gate. We denote by $UF \subseteq F$ the subset of faults which are detected by U . We perform fault collapsing based on the level of similarity starting from UF to obtain a set of collapsed faults CF . It is important to note that UF is already collapsed using the conventional approach. Thus, any additional collapsing we achieve will be on top of the conventional approach.

One of the metrics we will be interested in is the percentage reduction in the number of collapsed faults, or $|CF|/|UF| \cdot 100$. It is also possible to compute this percentage with respect to F by adding the faults in $F - UF$ (which are not considered by the proposed procedure) to CF and using $(|CF| + |F - UF|)/|F| \cdot 100$ as the per-

centage reduction in the number of collapsed faults. Since $F-UF$ is a very small subset of F in our experiments, this will not have a significant impact on the percentages reported. In many cases, $UF = F$.

5.1. Test selection

We are interested in obtaining test sets for several subsets of faults. (1) A test set CT for the set of collapsed faults CF obtained after applying fault collapsing to UF using similarity level SL_{MIN} , for different values of SL_{MIN} . (2) A test set UT for the set of faults UF . When CT detects all the faults in UF , we will be able to compare its size to UT since they detect the same set of faults. This will allow us to empirically evaluate whether the proposed fault collapsing method has any effect on the number of tests needed to detect all the faults obtained by using the conventional fault collapsing method.

We select a test set $T \subseteq U$ for a set of target faults $F_{targ} \subseteq UF$ using Procedure 2 given below. Procedure 2 considers the faults in F_{targ} one at a time. Initially $T = \emptyset$. For every fault $f \in F_{targ}$, Procedure 2 selects out of U the first test that detects f . The procedure adds t to T and drops from F_{targ} all the faults detected by t . At the end of Procedure 2, $F_{targ} = \emptyset$.

Procedure 2: Test selection

- (1) Let F_{targ} be the set of target faults and let U be the set of input vectors. Set $T = \emptyset$.
- (2) For every $f \in F_{targ}$:
 - Find the first vector $t \in U$ that detects f .
 - Add t to T and drop from F_{targ} all the faults detected by t .

Our goal is to find the smallest value of SL_{MIN} such that the test set CT , which is derived for the set of target faults CF obtained using SL_{MIN} , detects all the faults in UF . We achieve this goal by applying Procedure 3.

Procedure 3: Finding the smallest value of SL_{MIN}

- (1) Set $SL_{MIN} = 0.01$.
- (2) Call Procedure 1 to define a collapsed set of faults CF .
- (3) Call Procedure 2 with the set of target faults CF to define a test set CT .
- (4) Simulate UF under CT . If all the faults in UF are detected, stop.
- (5) Set $SL_{MIN} = SL_{MIN} + 0.01$ and go to Step 2.

Instead of increasing SL_{MIN} by 0.01, it is also possible to increase SL_{MIN} to the next value SL_{next} for which there is a fault pair f_i, f_j with $SL_{i,j} = SL_{next}$.

5.2. Results using U

In this subsection we report the results obtained when the set of input vectors U is used for computing the levels of similarity. We apply Procedure 3 to the combinational logic of MCNC finite-state machine benchmarks, and to the combinational logic of ISCAS-89 and ITC-99 benchmarks. We also apply the procedure to ISCAS-85 benchmarks, where a comparison is possible with the recent fault collapsing approach of [4], which is based on fault

equivalence and dominance. The results are reported in Tables 2, 3, 4 and 5 as follows.

Table 2: Using U for MCNC benchmarks

circuit	inp	U	UF	UT	SL	collapsing		%CT
						%CF	CT	
dk27	4	16	67	13	0.57	35.82	13	100.00
lion	4	16	40	11	0.71	40.00	10	90.91
shiftreg	4	16	28	7	1.00	42.86	7	100.00
train4	4	16	34	7	0.75	38.24	7	100.00
bbtas	5	32	63	13	0.56	34.92	13	100.00
dk15	5	32	151	22	0.55	23.18	22	100.00
dk17	5	32	128	21	0.53	24.22	21	100.00
dk512	5	32	124	24	0.53	31.45	24	100.00
ex5	5	32	152	24	0.53	23.03	23	95.83
lion9	5	32	62	15	0.55	35.48	15	100.00
mc	5	32	73	11	0.81	28.77	11	100.00
modulo12	5	32	68	15	0.56	39.71	14	93.33
beecount	6	64	110	22	0.53	29.09	20	90.91
dk14	6	64	207	29	0.53	26.09	27	93.10
ex3	6	64	153	28	0.51	25.49	27	96.43
ex7	6	64	159	34	0.72	30.82	32	94.12
s8	6	64	67	20	0.53	46.27	20	100.00
tav	6	64	64	16	0.71	39.06	16	100.00
train11	6	64	104	20	0.81	38.46	19	95.00
dk16	7	128	530	80	0.67	24.72	74	92.50
donfile	7	128	287	55	0.68	33.80	55	100.00
ex2	7	128	312	55	0.67	28.53	52	94.55
bbara	8	256	138	36	0.71	36.23	34	94.44
ex6	8	256	229	41	0.77	23.58	40	97.56
mark1	8	256	203	26	0.54	17.73	24	92.31
ex4	9	512	176	35	0.79	27.84	34	97.14
opus	9	512	181	34	0.67	33.15	33	97.06
bbsse	11	2048	238	50	0.67	29.41	50	100.00
cse	11	2048	355	67	0.67	27.61	64	95.52
keyb	12	4096	470	88	0.67	28.09	87	98.86
s1a	13	8192	632	115	0.84	31.17	111	96.52
dvram	14	16384	425	57	0.70	22.12	56	98.25
fetch	14	16384	342	51	0.83	23.39	48	94.12
log	14	16384	312	46	0.75	21.15	46	100.00
rie	14	16384	548	66	0.52	19.34	64	96.97
nucpwr	18	20000	447	46	0.71	21.70	46	100.00
average					0.66	30.07		97.10

Table 3: Using U for ISCAS-89 benchmarks

circuit	inp	U	UF	UT	SL	collapsing		%CT
						%CF	CT	
s386	13	8192	384	98	0.63	33.07	95	96.94
s1488	14	16384	1486	212	0.67	21.00	195	91.98
s208	19	20000	215	37	0.65	37.21	36	97.30
s298	17	20000	308	42	0.56	40.58	42	100.00
s344	24	20000	342	29	0.53	35.09	27	93.10
s382	24	20000	399	48	0.66	34.09	45	93.75
s400	24	20000	415	44	0.66	31.81	43	97.73
s420	35	20000	411	59	0.67	32.60	59	100.00
s444	24	20000	460	42	0.53	20.43	42	100.00
s510	25	20000	564	70	0.86	25.71	70	100.00
s526	24	20000	553	84	0.53	30.38	83	98.81
s641	54	20000	460	70	0.57	35.00	67	95.71
s820	23	20000	845	145	0.77	28.28	137	94.48
s953	45	20000	1073	108	0.78	20.04	107	99.07
s1196	32	20000	1203	153	0.56	20.45	145	94.77
s1423	91	20000	1499	101	0.78	31.95	100	99.01
average					0.65	29.86		97.04

After the circuit name we show the number of circuit inputs, the number of input vectors in U , and the number of faults detected by the input vectors in U (the size of UF). We then show the number of tests included in the test set UT computed by Procedure 2 for UF . Under column *collapsing* we show the following information for fault collapsing based on the level of similarity. Under subcolumn *SL* we show the value of SL_{MIN} for which all the faults in UF are detected (the value found

Table 4: Using U for ITC-99 benchmarks

circuit	inp	U	UF	UT	collapsing			
					SL	%CF	CT	%CT
b02	6	64	70	13	0.62	34.29	13	100.00
b01	8	256	135	26	0.68	32.59	26	100.00
b06	12	4096	202	30	0.51	24.26	30	100.00
b03	35	20000	452	38	0.60	40.93	35	92.11
b04	78	20000	1341	63	0.81	39.75	63	100.00
b09	30	20000	420	34	0.76	42.38	34	100.00
b10	29	20000	512	63	0.77	38.67	63	100.00
b11	38	20000	1074	84	0.67	28.58	83	98.81
average					0.68	35.18		98.86

Table 5: Using U for ISCAS-85 benchmarks

circuit	inp	U	UF	UT	SL	collapsing			[4]
						%CF	CT	%CT	%CF
c432	36	20000	520	62	0.76	40.00	63	101.61	85.69
c499	41	20000	750	62	0.40	12.00	59	95.16	93.14
c880	60	20000	942	70	0.62	44.06	69	98.57	-
c1355	41	20000	1566	89	0.30	6.96	88	98.88	76.87
c1908	33	20000	1870	148	0.84	31.07	142	95.95	83.34
c2670	233	20000	2321	85	0.53	25.46	87	102.35	84.35
c3540	50	20000	3289	190	0.87	36.09	191	100.53	81.27
c5315	178	20000	5291	160	0.82	39.73	158	98.75	83.96
c6288	32	20000	7710	42	0.56	18.12	41	97.62	75.21
c7552	207	20000	7155	208	0.73	18.91	201	96.63	81.22
average					0.63	29.75		98.80	85.01

by Procedure 3). Under subcolumn $\%CF$ we show the value of $|CF|/|UF| \cdot 100$, which is the percentage of faults out of UF included in CF for this value of SL_{MIN} . Under column CT we show the number of tests included in the test set CT computed by Procedure 2 for CF . Under column $\%CT$ we show the value of $|CT|/|UT| \cdot 100$.

In the last row of every table we show average values of SL_{MIN} , $|CF|/|UF| \cdot 100$ and $|CT|/|UT| \cdot 100$.

In the last column of Table 5 we show the percentage of faults included in the collapsed set of faults computed in [4]. This is the most recent fault collapsing procedure based on equivalence and dominance.

The following points can be seen from Tables 2, 3, 4 and 5. The value of SL_{MIN} for which all the faults in UF are detected is on the average 0.66 for MCNC finite-state machine benchmarks. Similar averages are obtained for the other benchmarks. These values indicate that the level of similarity does not have to be 1 to guarantee with a high probability the detection of all the circuit faults.

The size of CF is on the average 30.07% of the size of UF (which is collapsed by the conventional equivalence-based method) for MCNC finite-state machine benchmarks. Similar percentages are obtained for the other benchmarks. These values indicate the effectiveness of fault collapsing based on the level of similarity in aggressively reducing the set of target faults.

For ISCAS-85 benchmarks we can compare the relative size of CF to the one obtained in [4] using equivalence and dominance relations. It can be seen that fault collapsing based on the level of similarity allows significantly smaller sets of target faults to be obtained.

The test set CT selected for the collapsed set of faults based on the level of similarity is typically smaller than the test set UT selected by considering all the circuit faults. This indicates that the proposed fault collapsing

method leaves a set of faults whose tests are more likely to detect other, non-targeted faults.

5.3. Results using fanout free regions

In this subsection we report the results obtained when the levels of similarity are computed using fanout free regions. The results are reported in Tables 6, 7, 8 and 9 in the same format as before. We show averages in Tables 7 and 8 for the circuits also included in Tables 3 and 4.

Table 6: Fanout free regions for MCNC benchmarks

circuit	inp	U	UF	UT	collapsing			
					SL	%CF	CT	%CT
dk27	4	16	67	13	0.40	80.60	13	100.00
lion	4	16	40	11	0.60	80.00	10	90.91
shiftreg	4	16	28	7	1.00	71.43	7	100.00
train4	4	16	34	7	0.50	73.53	7	100.00
bbtas	5	32	63	13	0.33	74.60	13	100.00
dk15	5	32	151	22	0.14	63.58	22	100.00
dk17	5	32	128	21	0.38	71.09	21	100.00
dk512	5	32	124	24	0.57	75.81	24	100.00
ex5	5	32	152	24	0.55	76.97	24	100.00
lion9	5	32	62	15	0.60	80.65	15	100.00
mc	5	32	73	11	0.50	75.34	11	100.00
modulo12	5	32	68	15	0.50	69.12	14	93.33
beecount	6	64	110	22	0.33	74.55	22	100.00
dk14	6	64	207	29	0.22	66.18	30	103.45
ex3	6	64	153	28	0.50	73.20	28	100.00
ex7	6	64	159	34	0.60	79.87	34	100.00
s8	6	64	67	20	1.00	80.60	20	100.00
tav	6	64	64	16	1.00	79.69	16	100.00
train11	6	64	104	20	0.25	72.12	20	100.00
dk16	7	128	530	80	0.06	90.75	79	98.75
donfile	7	128	287	55	0.50	93.03	55	100.00
ex2	7	128	312	55	0.09	84.62	55	100.00
bbara	8	256	138	36	0.37	75.36	35	97.22
ex6	8	256	229	41	0.36	75.11	41	100.00
mark1	8	256	203	26	0.39	81.28	26	100.00
ex4	9	512	176	35	0.14	72.16	34	97.14
opus	9	512	181	34	0.50	78.45	33	97.06
bbsse	11	2048	238	50	0.25	71.85	50	100.00
cse	11	2048	355	67	0.05	71.27	65	97.01
keyb	12	4096	470	88	0.36	82.13	88	100.00
s1a	13	8192	632	115	0.45	89.56	115	100.00
dvrarn	14	16384	425	57	1.00	79.53	57	100.00
fetch	14	16384	342	51	0.33	88.01	51	100.00
log	14	16384	312	46	0.07	78.85	46	100.00
rie	14	16384	548	66	0.09	83.94	67	101.52
nucpwr	18	20000	447	46	0.33	82.10	46	100.00
average					0.43	77.69		99.34

The following points can be seen from Tables 6, 7, 8 and 9. The most noticeable difference from Tables 2, 3, 4 and 5 is that the percentage of faults included in the collapsed fault set CF is higher when fanout free regions are used for computing the levels of similarity than when levels of similarity are computed based on a set of vectors U . This is due to the following effect. When the set of input vectors U is used, we can potentially associate a non-zero level of similarity with every pair of faults. When considering fanout free regions, only faults in the same fanout free region can have a non-zero level of similarity. The fault pairs with level of similarity equal to zero cannot contribute to fault collapsing. As a result, with fanout free regions we have fewer faults that can contribute to fault collapsing, and CF is larger.

Nevertheless, we obtain non-trivial reductions in the size of CF even when fanout free regions are used. For

Table 7: Fanout free regions for ISCAS-89 benchmarks

circuit	inp	U	UF	UT	collapsing			
					SL	%CF	CT	%CT
s386	13	8192	384	98	0.36	82.03	97	98.98
s1488	14	16384	1486	212	0.18	94.21	211	99.53
s208	19	20000	215	37	0.50	83.26	37	100.00
s298	17	20000	308	42	0.80	77.92	41	97.62
s344	24	20000	342	29	1.00	71.93	29	100.00
s382	24	20000	399	48	0.40	72.18	48	100.00
s400	24	20000	415	44	0.40	70.36	44	100.00
s420	35	20000	411	59	0.33	79.08	59	100.00
s444	24	20000	460	42	0.12	69.13	42	100.00
s510	25	20000	564	70	0.09	78.19	70	100.00
s526	24	20000	553	84	0.34	76.85	84	100.00
s641	54	20000	460	70	0.08	76.74	69	98.57
s820	23	20000	845	145	0.20	93.37	145	100.00
s953	45	20000	1073	108	0.42	78.75	108	100.00
s1196	32	20000	1203	153	0.60	83.71	153	100.00
s1423	91	20000	1499	101	0.75	65.31	101	100.00
average					0.41	78.31		99.67
s5378	214	20000	4540	316	0.50	85.48	316	100.00
s9234	247	20000	5947	346	0.52	80.11	346	100.00
s13207	700	20000	9371	483	0.68	78.86	481	99.59
s15850	611	20000	10788	369	0.68	75.11	371	100.54
s35932	1763	1000	35110	67	1.00	67.25	68	101.49
s38417	1664	20000	27046	367	0.60	70.52	366	99.73
s38584	1464	20000	34439	834	0.57	67.14	829	99.40

Table 8: Fanout free regions for ITC-99 benchmarks

circuit	inp	U	UF	UT	collapsing			
					SL	%CF	CT	%CT
b02	6	64	70	13	0.14	60.00	13	100.00
b01	8	256	135	26	0.53	68.15	26	100.00
b06	12	4096	202	30	0.50	71.78	30	100.00
b03	35	20000	452	38	0.45	75.88	38	100.00
b04	78	20000	1341	63	0.50	74.27	63	100.00
b09	30	20000	420	34	0.50	78.33	34	100.00
b10	29	20000	512	63	0.57	78.32	63	100.00
b11	38	20000	1074	84	0.50	70.95	84	100.00
average					0.46	72.21		100.00
b14	280	20000	8213	206	0.78	82.04	206	100.00
b20	527	20000	19524	358	0.52	79.46	358	100.00

Table 9: Fanout free regions for ISCAS-85 benchmarks

circuit	inp	U	UF	UT	collapsing			
					SL	%CF	CT	%CT
c432	36	20000	520	62	1.00	90.38	62	100.00
c499	41	20000	750	62	0.50	45.60	58	93.55
c880	60	20000	942	70	1.00	71.87	70	100.00
c1355	41	20000	1566	89	0.50	62.71	89	100.00
c1908	33	20000	1870	148	1.00	72.19	148	100.00
c2670	233	20000	2321	85	0.36	75.87	85	100.00
c6288	32	20000	7710	42	0.50	63.06	42	100.00
c7552	207	20000	7155	208	1.00	70.51	207	99.52
average					0.73	69.02		99.13

MCNC finite-state machine benchmarks, the size of CF is on the average 77.69% of the size of UF .

5.4. Summary

As discussed earlier, the level of similarity $SL_{i,j}$ is one when f_j is equivalent to f_i or when f_j dominates f_i . Thus, fault collapsing based on the level of similarity with $SL_{MIN} = 1$ is identical to fault collapsing based on equivalence and dominance relations. With $SL_{MIN} < 1$, additional fault collapsing will occur.

The comparison with the results from [4] indicates that collapsing based on the level of similarity can provide significantly higher levels of reductions in the number of target faults than existing approaches.

From the experiments reported in Subsections 5.2 and 5.3, we obtain collapsed sets of faults that are around 30% of the conventional collapsed sets when levels of similarity are computed based on sets of input vectors, and around 75% when they are computed based on fanout free regions. This indicates that there is significant room to develop efficient methods for computing the level of similarity that will achieve high levels of fault collapsing.

6. Concluding remarks

We described a new approach to fault collapsing based on the level of similarity between faults. A fault f_j is said to be similar to a fault f_i with a level of similarity $SL_{i,j} \leq 1$ if a fraction $SL_{i,j}$ of the tests for f_i also detect f_j . If $SL_{i,j}$ is high enough, one may exclude f_j from the set of target faults and rely on the test for f_i to detect f_j as well. Fault collapsing based on the level of similarity extends the earlier approaches to fault collapsing based on fault equivalence and fault dominance. Specifically, fault collapsing based on the level of similarity reduces to fault collapsing based on fault equivalence and fault dominance when only faults with level of similarity one relative to faults in the set of target faults are excluded from the set of target faults. We described a procedure for fault collapsing based on the level of similarity, and studied its effectiveness experimentally. In particular, we identified a minimum level of similarity that allows us to perform fault collapsing based on the level of similarity without losing fault coverage in benchmark circuits.

References

- [1] K. To, "Fault Folding for Irredundant and Redundant Combinational Circuits", IEEE Trans. on Computers, 1973, pp. 1008-1015.
- [2] M. Abramovici, M. A. Breuer and A. D. Friedman, *Digital Systems Testing and Testable Design*, Computer Science Press, 1990.
- [3] R. Hahn, R. Krieger and B. Becker, "A Hierarchical Approach to Fault Collapsing", in Proc. European Design and Test Conf., March 1994, pp. 171-176.
- [4] A. V. S. S. Prasad, V. D. Agrawal and M. V. Atre, "A New Algorithm for Global Fault Collapsing into Equivalence and Dominance Sets", in Proc. Intl. Test Conf., Oct. 2002, pp. 391-397.
- [5] V. D. Agrawal, "Sampling Techniques for Determining Fault Coverage in LSI Circuits", Journal of Digital Systems, 1981, pp. 189-202.
- [6] V. D. Agrawal, H. Farhat and S. Seth, "Test Generation by Fault Sampling", in Proc. Intl. Conf. on Computer Design, Oct. 1988, pp. 58-61.
- [7] S. A. Al-Arian and M. A. Al-Kharji, "Fault Simulation and Test Generation by Fault Sampling Techniques", in Proc. Intl. Conf. on Computer Design, Oct. 1992, pp. 365-368.