VHDL-AMS Library Development for Pacemaker Applications

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Abstract

This paper describes the development by ELA Medical of an analog library dedicated to implantable pacemakers and defibrillators using the VHDL-AMS language for mixed-signal ASICs. ELA Medical has been a leading company since 1977 for medical devices used in the diagnosis and treatment of heart rhythm disorders. The objective is to provide designers with a ready-to-use customized library for mixed-signal top-down and bottom-up methodologies. The dramatic gain in simulation speed by using behavioral models allows more exhaustive functional validation within an acceptable simulation time. The ADMS mixed-signal simulator from Mentor Graphics has been used with design kit environments provided by major silicon vendors.

1. Introduction

The ever-increasing levels of integration complexity of ASICs in general, and the need to include more and more complex analog and digital functions, combined with extremely low power consumption requirements, have urged ELA Medical to reconsider its existing ASIC design methodologies for implantable pacemakers and defibrillators. The traditional mixed-signal validation methodology is based on analog kit parts in the target technology driven by digital FPGAs. Although such hardware validation is very complete, the drawback is time consuming due to the design and the fabrication delay. Co-simulation with Spice has also been used at different levels but such a solution still faces limitations in many cases due to the prohibitive simulation time.

The new generation single-kernel mixed-signal simulators (such as ADMS from Mentor Graphics) is language-neutral and allows designers to freely combine VHDL, Verilog, VHDL-AMS, Verilog-AMS, SPICE and C anywhere in their designs to trade-off between accuracy and detail effects vs. speed performance. In best cases, the new approach can speed up the simulation time until 30X. However, to adopt such a new methodology ELA Medical has to develop a specific behavioral library for its new MOSAIC ASIC project including other very sensitive discrete device models such as transformers and inductors.

Adopting such a new methodology not only requires significant effort to build-up the library but also to train designers on tools and new approaches in the middle of the project. Once designers are trained and the low power and low voltage custom library is ready, ELA Medical aims to improve its productivity by shrinking the design cycle time and producing higher performance medical devices.

2. MOSAIC Project

An ICD (Implantable Cardioverter Defibrillator) is a pacemaker with additional hardware and software functionality necessary to deliver the appropriate electrical shocks. Similar to pacemaker specifications, ICD should meet drastic size and pricing requirements, which call for very tight power consumption control and a high level of circuit integration. In addition, ICD design deals with high power and high current, which requires different battery technology from the one used by a pacemaker. To meet such a challenge, ELA Medical is currently working on the MOSAIC project to design a special mixed-signal ASIC, which is an interface circuit that includes stored energy management capable of delivering an electrical shock of 30 Joules.

The main function of MOSAIC is to provide, from a battery, both a permanent power supply for the low power circuit and a monitored power supply and control signals for the high current circuit needed by the defribillator. The design is completely controlled by a state machine and can only be validated in a mixed-signal simulation environment. Simulation speed performance is critical in order to obtain all the required test figures. ELA Medical has decided to develop analog behavioral models to speed up simulation run time. Another important objective is to

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reduce the number of discrete components used in the system. In this case, behavioral models allow designers to experiment alternative architectures.

Fig 1. Dual chamber ICD

3. VHDL-AMS Library Development

Although commercial libraries ars available, such as CommLib from Mentor Graphics, but they do not completely meet our specific requirements in power management. Since a defibrillator remains, fortunately, mostly inactive, the models should take into account the behavior of both configurations when the power supply is on and off. Also, each model must include an additional output to provide power consumption estimation.

The library development is done in collaboration with EFREI. Most models have several levels of abstraction. Each VHDL-AMS model has an associated validation testbench. Finally the library is completely integrated into our IC design flow and is now available to designers for the MOSAIC project.

4. Design Methodologies

The introduction of VHDL-AMS models in our mixed-signal ASIC top-down design cycle has a "V" shape as follows:

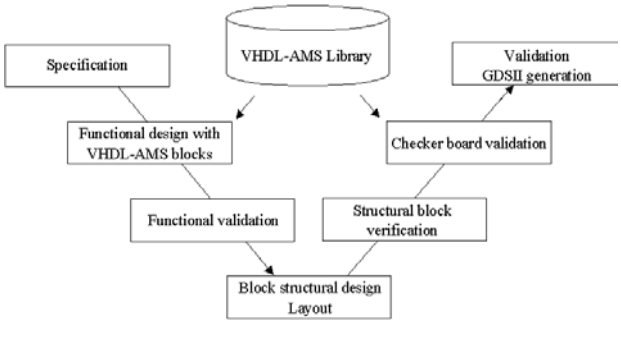

Fig 7. Design Methodology

Following specifications, each block is represented by a VHDL-AMS functional model to allow virtual prototyping and to fine-tune the specifications before moving to the implementation. Designers then develop the circuit at the structural representation and physical layout of each block followed by block level verification. The complete structural level validation is achieved by successively replacing each VHDL-AMS block at a time by its equivalent circuit. As a result, faster simulation time is achieved when the design is broken down into smaller blocks, since the rest of the design remains at the functional level. Today our VHDL-AMS library has made full-chip verification a reality.

The library has been valided on our actual most critical applications, a DC-DC converter. The switching voltage regulato, optimized by a state machine, includes also external components such as battery, inductor and storage capacitor. We display below a comparison of simulation results between transistor level (on top) and behavioral level (bottom). Due the differences in comparator delay time, the waveforms are shifted to the right. But globaly the results remained identical.

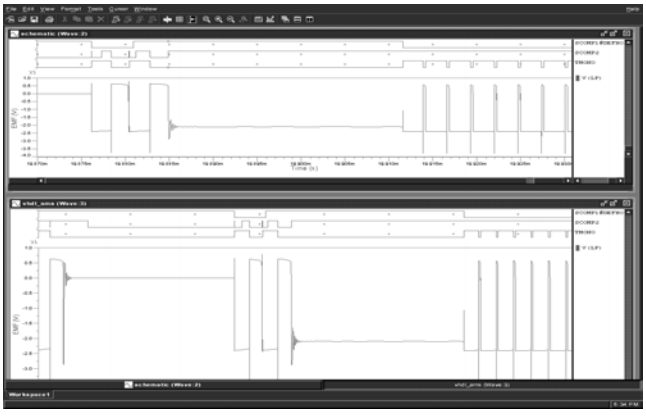

Fig 10. Converter simulation results

5. Conclusion

The completeness of our VHDL-AMS library together with the mixed-signal simulator ADMS from Mentor Graphics has allowed us to validate the new complex architectures of our design. The great improvement in speed performance of the new methodology (compared with traditional tools) enables us to optimize ASIC power consumption more quickly and allows greater scope for innovation. Finally, in a top-down approach, the parameterized analog behavioral models of our library can be used to fine-tune the block specifications before final implementation.