A CAD Methodology and Tool for the Characterization of Wide On-chip Buses

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Abstract: *In this paper, we describe a CAD methodology for the full electrical characterization of high-performance, on-chip data buses. The goal of this methodology is to allow the accurate modeling and analysis of wide, on-chip data buses as early as possible in the design cycle. The modeling is based on a manufacturing (rather than design-manual) description of the back-end-of-the-line (BEOL) cross section of a given technology and on a full yet contained description of the power-ground mesh in which the data bus is embedded. One major aspect of the resulting electrical models is that they allow the designer to evaluate the wide bus from the three viewpoints of signal timing, crosstalk (both inductive and capacitive), and common-mode signal integrity. Another major aspect is that they take into account such important high-frequency phenomena as the dependence of the current return-path resistance on frequencies. The CAD methodology described in this paper has been extensively correlated with on-chip hardware measurements.*

1 Introduction

In [1], we have described AQUAIA (All Questions About Interconnect Answered), a new CAD tool for the modeling, analysis and optimization of on-chip interconnect. The basic premise of the AQUAIA methodology is that *all* relevant interconnect behavior, including frequency-dependent resistive and inductive effects, can be efficiently and accurately captured using well-defined, self-contained interconnect structures. The definition of these interconnect structures is based on the power/ground mesh layout while their extent (e.g., number of same-layer power bays, number of metal layers below and above, etc.) is determined by the physics of current path distribution in the combined power/signal structure. One important consequence of this methodology is that global on-chip signal lines can be efficiently modeled as wideband $R(f)L(f)C$ multiconductor transmission lines (MTL). These MTL models have been extensively validated by measurements on actual on-chip test sites [2, 3, 4] and are known to have compact SPICE circuit models [5, 6, 7] that allow them to be reliably analyzed with SPICE-level simulators.

In this paper, we describe how the AQUAIA methodology can be extended to enable the full characterization of on-chip, wide data buses. The fundamental feature of on-chip data buses is that their geometric layout is spread over multiple power bays. This layout introduces a number of complications at both the extraction and simulation levels. One such complication at the extraction level is that parametric capacitance and $R(f)L(f)$ extraction becomes time-consuming even in the 2D case. Furthermore, some of the "mutual" $R_{ij}(f)$ and $L_{ij}(f)$ exhibit non-monotonic behavior that is quite challenging to represent with compact circuit models.

Our main goal in extending AQUAIA's capabilities to wide on-chip data buses is to seamlessly automate the extraction, modeling and simulation flow of these structures so as to enable interconnect designers to quickly evaluate design alternatives from the viewpoints of layout, timing, and signal integrity. Another major goal of this automation is to enable designers who are not versed in the characterization of wideband $R(f)L(f)C$ wire models to use these models in their design practice as they are the only ones capable of capturing common-mode noise which is a long-range, wideband signal integrity phenomenon induced by the simultaneous switching of the bus drivers [2, 3, 8, 4]. Section 2 of this paper discusses previous work related to ours. Section 3 gives a description of the overall bus characterization methodology which includes the three essential steps of paramater extraction, electrical modeling, and circuit simulation. Section 4 addresses the wideband $R(f)L(f)$ parameter extraction process for wide data buses, while Section 5 deals with the challenges of wide, on-chip bus electrical modeling. Finally, Section 6 presents results pertaining to the analysis of signal integrity in a 12-line data bus for both the shielded and unshielded case.

2 Related Work

It is important to stress that the methodology we propose is one of interconnect characterization and exploration. The tool that embodies this methodology is geared toward prelayout, accurate, custom interconnect modeling. It is not geared toward post-layout, full-chip extraction and verification. Like technology exploration systems, such as GENESYS [9], RIPE [10], BACPAC [11], and GTX [12], AQUAIA uses technology and user inputs to explore the BEOL design space. But unlike these exploration systems which rely on approximate delay and noise formulas, AQUAIA rely on the accurate modeling of interconnect

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structures to derive reliable figures of merit for interconnect performance. An important byproduct of the tool is a SPICE-level macromodel of a variety of on-chip interconnect structures, including clock nets, signals nets, IO nets, and global buses.

Regarding the latter structures, [13] gives a careful analysis of the impact of inductance on the electrical performance of on-chip buses. Important design issues such as bus shielding and buffering are considered. The interesting results obtained are however restricted to *RLC* bus models rather than the more accurate $R(f)L(f)C$ models. One of the major goals of our methodology and tool is to provide parameterized $R(f)L(f)C$ SPICE-level models for wide on-chip data buses. The work described in [14] provides such parameterized models for the stripline and microstrip transmission lines arising in the RF/mixed-signal design context. These structures do not arise in the digital CMOS context, and their models are of limited use from the viewpoint of signal integrity in wide, on-chip data buses. In a recent paper, [15] analyzed the impact of $R(f)L(f)C$ models on the signal integrity in on-chip signal nets. The analysis used low-order ladder networks to efficiently model the $R(f)L(f)$ dependence on frequency. The observation of [15] that such models are crucial to capture signal integrity phenomenon in global on-chip interconnect structures is fundamentally correct and is in agreement with our own observations and observations made much earlier in [2] and the references therein. However the models in [15] do not include the dependence of the return-path resistance on frequency, and only DC mutual inductance between bus nets are taken into account. Such restrictions do not exist in our electrical models.

3 On-chip Bus Characterization

The key idea of our on-chip bus characterization methodology is to to use what we call interconnect *motifs* to enable the accurate extraction of capacitance and series impedance parameters. The main reason such motifs can be accurately described is that in high-performance designs, the structure of the power-ground mesh at all metal levels is a given in the global interconnect design process (clock, bus, or IO nets). Unlike other technology exploration tools, we make use of this knowledge to build the minimum interconnect environment required for the accurate extraction of the bus electrical parameters.

One can think of the on-chip bus motif as a data structure containing the following elements:
BEOL elements: Bus metal layer name and thickness, metal layer dielectric constant; via layers above and below (structure, thickness, and dielectric constants).
Bus elements: Number of bitlines and their distribution among the power/ground bays containing the bus; bitline width, pitch, and spacing between bitline and power/ground line; in the presence of shielding, shield line width and spacing between shield and bitline.
Power mesh elements: Power line width and pitch; and for the top layer, C4 (solder balls) pads pitch and width.
Model elements: For 3D capacitance, interconnect loading densities in the orthogonal metal layers immediately below and above the bus line; power mesh pitch and spacing in the orthogonal metal layers immediately below and above the bus; and for 2D and 3D inductance, power mesh pitch and spacing in the parallel metal layers immediately below and above the bus layer.

These elements are all relevant to the proper parameterization of bus electrical models. One future direction for this work is to use AQUAIA as the backbone for the generation of parameterized library cells for on-chip interconnect motifs.

Another important ingredient of the bus characterization methodology is the knowledge that signal nets running in parallel within power bays can be quite accurately modeled as a multiconductor transmission line system [3]. This observation, which is based on a significant body of experimental data [3, 4], has important consequences regarding the bus electrical parameter extraction and SPICE-level macromodeling.

Figure 1(a) shows the overall structure of AQUAIA. The primary input is a technology file containing an accurate description of the CMOS technology BEOL cross section as well as the wire pitch and width of the power mesh in each metal layer. The AQUAIA core engine uses this technology file along with user inputs (number of bitlines, parameter names and ranges, circuit parameters, etc.) to extract the per-unit-length (PUL) parameters of the signal lines and to automatically generate SPICE netlists containing the full electrical model of the interconnect structure. The tool then runs these netlists and computes the electrical performance parameters (e.g. delay, crosstalk) that fully characterize the interconnect structure under consideration. AQUAIA is structured so as to allow matrix parametric simulations of any combination of variables, be they technology (e.g., dielectric constant), geometric (e.g., power mesh pitch), or electrical variables (e.g., beta ratio of drivers and receivers). This makes AQUAIA an ideal integrated extraction and simulation environment for evaluating the BEOL technology parameters in the pre-design-manual phase and exploring the interconnect design space in the pre-layout phase.

Once the interconnect motif is built, a series of bus electrical models of increasing accuracy can be generated by the tool. The flowchart for model generation is shown in Figure 1(b).

As shown in Figure 1(a), AQUAIA has an intuitive, easy-to-use graphical user interface based on the Qt^{TM} widget set.[1]

4 Wideband Extraction

To illustrate the bus characterization flow, we use a 12-line bus running in 3 power bays on the top metal layer of a state-of-the-art copper BEOL stack, Figure 3(c). The power mesh pitch is 11.2 μm and the power line width is 2.4 μm. The signal wire pitch is 1.6 μm and its width is 0.8 μm. The metal thickness of the layer is 1.2 μm. Figure 2(a) shows the geometry used for the 2D capacitance extraction. One important feature of this geometry is that it includes all the dielectric details of the BEOL cross section. These details are derived directly from the BEOL process technology file rather than the design manual. Figure 2(b) shows the geometry used for the wideband extraction of $R(f)$ and $L(f)$. Note that one power bay was added on each side of the bus. Furthermore, the power mesh of the bottom metal layer parallel to the top layer has been added to the signal layer power mesh. The side power bays as well as the bottom parallel power bays are included to capture the spreading of return current at low frequencies. Furthermore, since the top metal layer contains the C4 straps that transfer power from the package to the chip, two C4 straps have been added around the bus. In this example, the C4 pitch was 455 μm and the width of the C4 strap is 55 μm. These C4 paths provides low-resistance return paths for the current at very low frequencies. Their inclusion is essential for capturing the low-frequency behavior of the return-path impedance. Figure 2 corresponds to an unshielded bus. When grounded wires are placed in the middle of each power bay, the 12-line bus will have the capacitance and impedance extraction structures shown in Figure 3 (a) and (b), respectively (the C4 pads are not shown for lack of space). All these extraction structures enable the computation of $R(f)L(f)$ parameters over very wide frequency ranges. A typical range used in AQUAIA is 1KHz to 100GHz. The result of the capacitance extraction is a 12×12 matrix containing the PUL capacitances of the bus considered as a an MTL structure. One observation about this matrix is that it is almost block diagonal with, for the unshielded case, three blocks corresponding to the 4×4 capacitance matrices of the signal lines in the individual power bays. This is because of the capacitive shielding due to the power/ground mesh. On the other hand, the frequency-dependent PUL coefficients of 12×12 inductance matrix are slowly decreasing functions of the distance between signal lines. This can be clearly seen in Figure 3 where the loop self inductances (a) the 2nd-nearest-neighbor mutuals (b) and the 9th-nearest-neighbor mutuals (c) have only a 3X variation range.

5 Electrical Modeling

The major difficulty in finding a robust, efficient electrical model of a wide data-bus is evident in Figures 4 and 5. Figure 4(a) shows the classical monotonic behavior of direct resistances as function of frequency. Similarly, Figure 5(a) shows that the self inductances are decreasing functions of frequency. This monotonic behavior is what to be expected whenever the signal lines are running in a single power bay and the EM interactions between their currents do not involve any return-path sharing. However, as soon as the signals are spread over several power bays as is the case for wide buses, the dependence of PUL return-path resistance and PUL mutual inductance on frequency becomes non-monotonic. Figure 4(b) shows how the return-path PUL resistance of signal line pairs (3,5), (4,6), (7,9) and (8,10) becomes non-monotonic (counting bitlines from the bottom in Figure 3(c)). This non-monotonic behavior is shown more clearly in Figure 4(c) for signal line pairs that are 9-th nearest neighbors, namely (1,10), (2,11), and (3,12). Another unique feature of the parameters of wide data buses is the existence of frequency ranges over which the magnetic coupling between signal lines becomes negative as is clear from Figure 5(c) where the mutual inductance becomes negative around the 1GHz range. The shielded bus case exhibits a noticeably more negative mutual inductance than the unshielded case. This negative mutual inductance is a physical phenomenon that expresses the fact that current flowing in the magnetically coupled circuit has the opposite polarity of the current flowing in the primary circuit. One very simple situation where such current inversion occurs is shown in Figure 6(a) where the power lines are sandwiched between the signal lines, which results in the two coupled circuits sharing magnetic flux through the surface area extending between the two power lines, especially at very low frequencies. Figure 6(c) shows that indeed the mutual inductance is negative over the low-frequency range and becomes positive only when the return current crowds in the neighborhood of the signal conductors at high frequencies.

6 Simulation

Despite the above difficulties, our work has shown that it is possible to come up with compact, reliable models of $R(f)L(f)C$ bus structures. One such compact model is the one presented in [3, 5]. Another compact model we have implemented is the one based on [6]. Such models can be incorporated in SPICE netlists and simulated along with the driving and receiving (nonlinear) buffer banks. In the example of this paper, the line length is 4mm, and the quiet bit line, the 7th from the bottom, Figure 3(c), is assumed to be held at VDD = 1 volt. From the viewpoint of signal integrity, the worst-case input vector is one in which all the

[1] Qt is a trademark of Trolltech. A subset of Qt is part of the open source software on the Linux platform.

active lines are switching simultaneously with the two lines closest to the quiet net having a switching polarity opposite (low to high) to the other active lines (high to low). All active lines are switching with a 50ps transition time. Figure 7 shows the results of running SPICE on the netlist containing drivers, receivers and the bus $R(f)L(f)C$ model. Each plot shows two waveforms at the far ends of lines 1, 6, and 7 (quiet). The first waveform is for an RLC model (no dependence on frequency) and the second waveform is for the $R(f)L(f)C$ model. It is clear from Figure 7(c) that extracting *only* high-frequency inductance does not account for the full noise waveform. In fact noise would be underestimated by about 20%. Another set of SPICE simulations is presented in Figure 8 where the shielded bus is compared with the unshielded one. One important observation is that shielding does reduce the noise on the quiet line. However this reduction is due mostly to lower capacitive coupling in the shielded case. Noise due to inductive coupling and coupling due to return-path sharing (common-mode noise) is still present.

7 Conclusions

We have presented a methodology and tool for the characterization of wide on-chip buses. Some of the problems unique to these structures (return-path sharing, negative mutual inductance, non-monotonic return-path resistance as function of frequency) have been emphasized possibly for the first time in the CAD literature. These problems have been overcome, and as a result, reliable, robust $R(f)L(f)C$ electrical models for on-chip buses can now be generated and used in a pre-layout context to define the wide bus design ground rules for avoiding inductive, capacitive and common-mode noise. The generation of *parameterized* on-chip bus models and their use for the optimization of on-chip bus structures for performance, throughput, and signal integrity will be addressed in a future paper.

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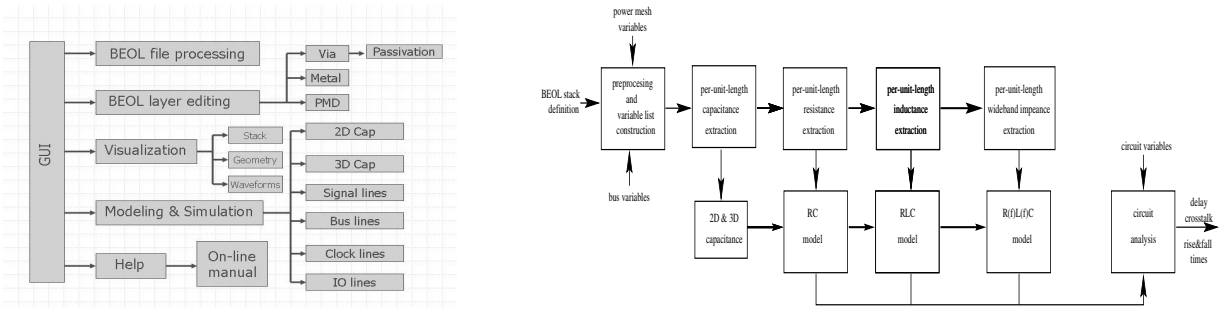
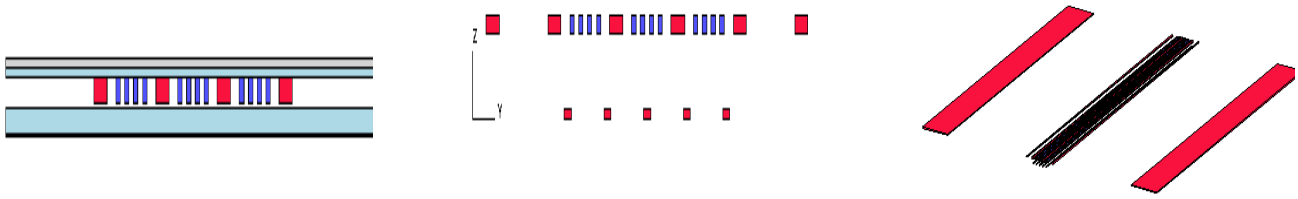


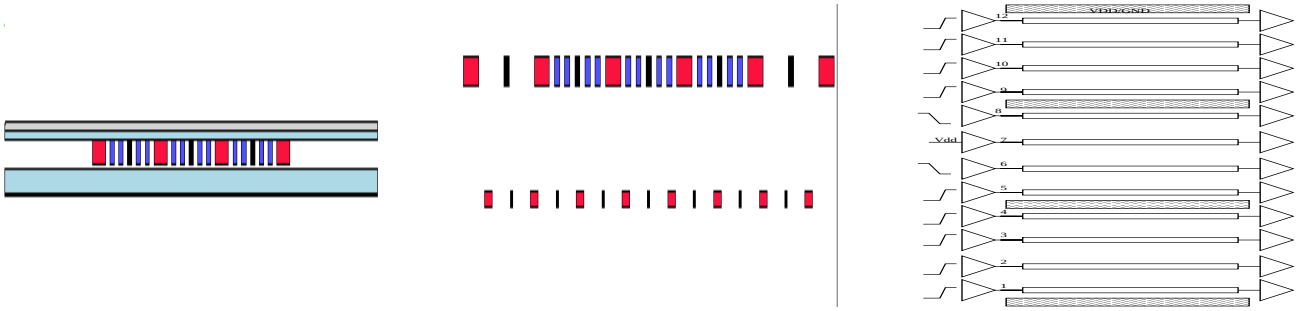
(a) (b)

Figure 1: (a) On-chip interconnect tool organization. (b) Bus model generation flow.



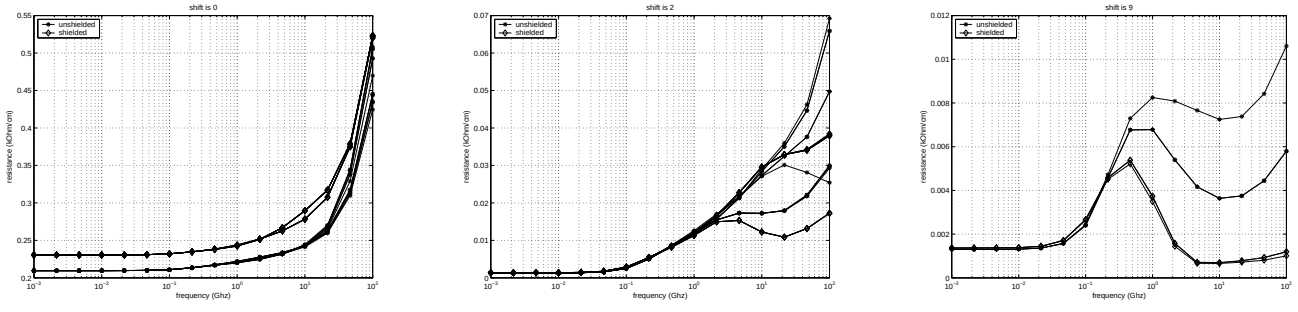
(a) (b) (c)

Figure 2: Extraction geometries (unshielded): (a) capacitance (b) wideband impedance (c) C4 pads for wideband impedance. Blue: bitline. Red: power line. Black: shielding wire.



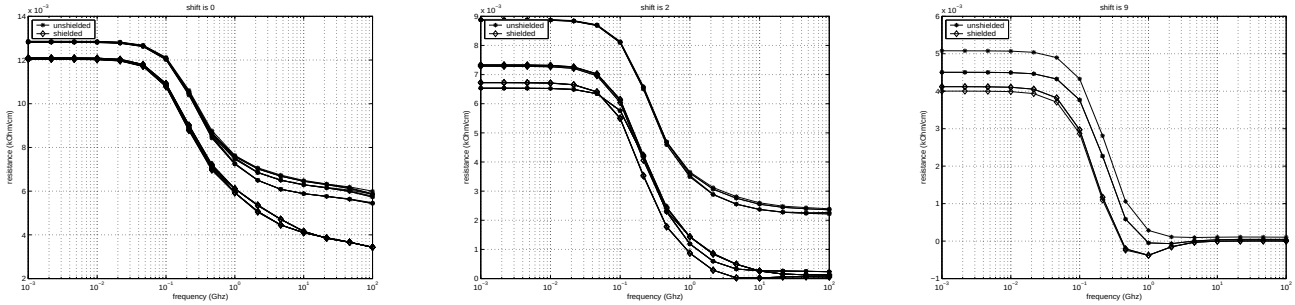
(a) (b) (c)

Figure 3: Extraction geometries (shielded): (a) capacitance (b) wideband impedance (c) 12-line bus schematics and input signal polarities.



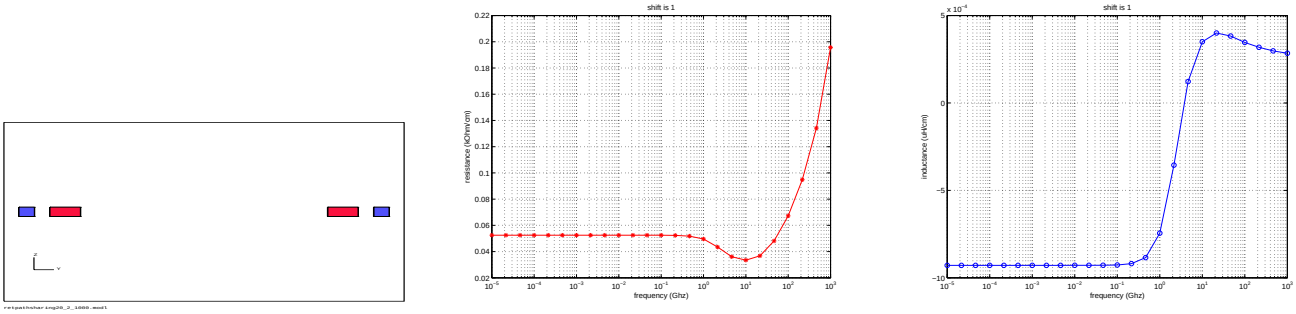
(a) (b) (c)

Figure 4: Frequency-dependent per-unit-length resistance: (a) “self” resistance (b) return-path resistance for 2nd nearest neighbors and (c) 9-th nearest neighbors .



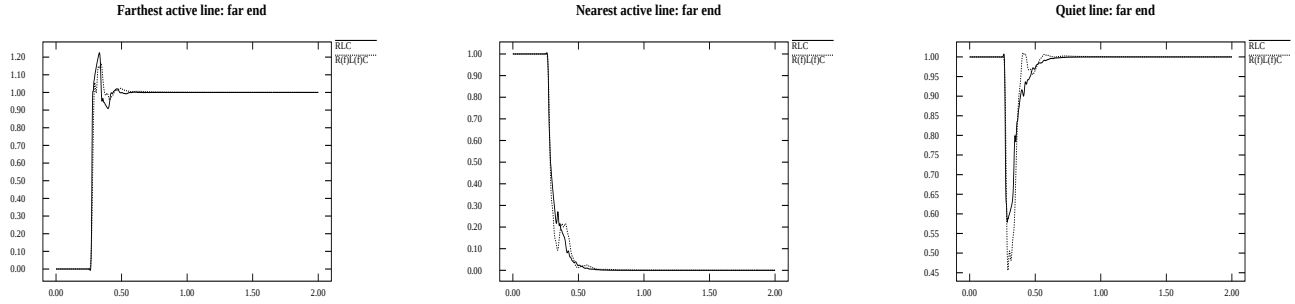
(a) (b) (c)

Figure 5: Frequency-dependent per-unit-length inductance: (a) self inductance (b) mutual inductance for 2nd nearest neighbors and (c) 9-th nearest neighbors .



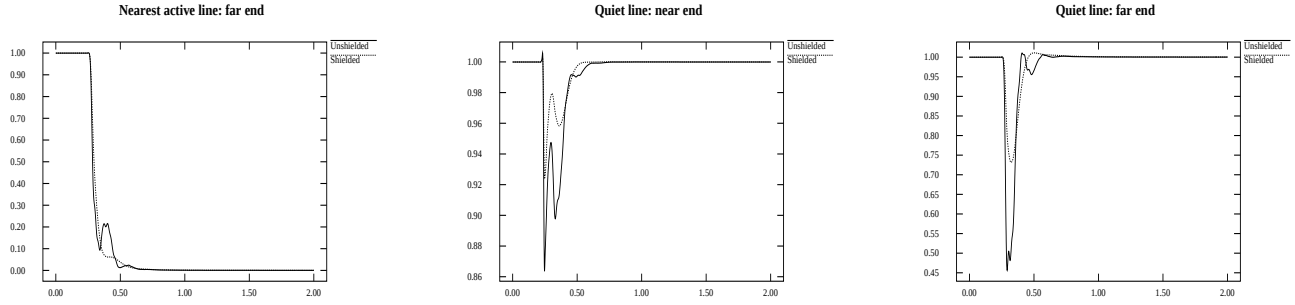
(a) (b) (c)

Figure 6: Return-path sharing and negative mutual inductance (a) structure: signal lines are 1×1 μm, power lines are 2×1 μm, signal-to-power spacing is 1μm, power spacing is 16 μm; (b) non-monotonic return path resistance (c) non-monotonic mutual inductance; note the negative mutual inductance at low frequencies.



(a) (b) (c)

Figure 7: SPICE simulation of the unshielded 12-line bus: comparing *RLC* and $R(f)L(f)C$ (a) farthest active line (b) closest active line (c) quiet line.



(a) (b) (c)

Figure 8: SPICE simulation of the shielded 12-line bus (a) nearest active line: far end (b) quiet line: near end (c) quiet line: far end.