An Inductance Modeling Flow Seamlessly Integrated in the RF IC Design Chain

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Abstract

A novel design flow is introduced based on an efficient inductance modeler, supporting RLCk extraction for spiral inductors, transformers and RF interconnect lines. The modeler operates on a set of EM-derived algorithms that can model complex cross-coupled devices on any silicon substrate rapidly and reliably. A design flow is set up in Cadence SKILL, integrating the inductance modeler with the layout editor and RCX extraction tools. Spiral inductor parametric cells are provided, that can be extracted with full connectivity in a single netlist along with other layout devices and parasitics. The resulting netlist includes mutual coupling (k) elements and is produced automatically without need for user intervention or back-annotation. Measured results on RF silicon circuitry showcase the accuracy and efficiency of the inductance modeling flow. The introduced flow can evolve into a platform for RF Intellectual Property (IP) evaluation and trade.

1. Introduction

In the past decade two major trends have made imperative the need for efficient and accurate modeling of inductance, both as a parasitic and as an intentional element of silicon integrated circuits: multi-gigahertz processors and highly integrated transceivers for wireless, RF and optical applications.

Integrated spiral inductors, broadly used in today's RF IC designs, are usually characterized in terms of their inductance (L) and quality factor (Q) values. They also exhibit a self-resonance frequency above which a spiral becomes useless (Figure 1). Inductors integrated on the same die also present mutual inductance effects that alter their performance. Unless this behavior is properly analyzed and modeled, RF IC design becomes more of a 'black art' rather than a systematic process. Although today several 2.5D and 3D electromagnetic (EM) simulation tools succeed in modeling accurately on-chip and in-package inductances, there is still no available solution that can address simultaneously the needs for short design cycles, high accuracy, IC design flow integration and rapid circuit optimization enablement. More specifically, the lack of an integrated flow built within a standard RF IC design chain forces designers to either rely on pre-characterized – usually restricted – libraries of inductive components or to revert to EM solvers which, though accurate, typically take hours to compute the performance of even simple inductor structures.

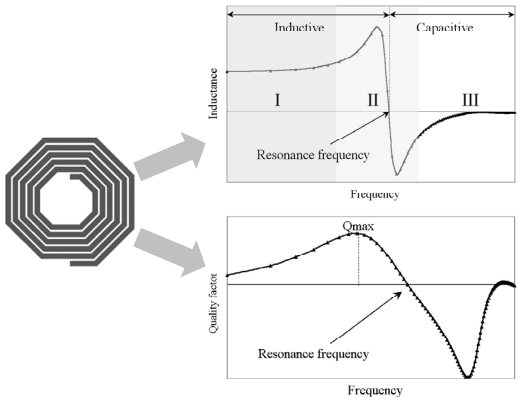

Figure 1. Beyond their resonance frequency, spiral inductors become capacitors

In this paper, a novel RF IC design flow is introduced based on an efficient inductance modeler that supports the extraction of detailed RLCk netlists for spiral inductors, transformers, arbitrarily-shaped inductive elements and RF interconnect lines in general. The modeler operates on a set of EM-derived algorithms which are extremely rapid and scaleable and can support complex cross-coupled devices on any silicon substrate, with an overhead of only few seconds on top of the typical RC extraction process.

The proposed flow (dubbed VeloceRF) can enable whole-chip RF simulation, closing the gap of inductance modeling in the RF IC design chain. Experimental silicon has proven its accuracy with first-pass successes. The flow promises to slash RF IC development cycles and related non-recurring engineering expenditures for typical RF transceiver development projects. Die area and related variable silicon costs may also be reduced, as a consequence of the ability to design custom inductors, optimize them for a given area and lay them out in close proximity to each other.

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2. Inductor modeling engine

The inductor modeling engine behind VeloceRF was originally based on [1] but was later enhanced with several proprietary algorithms. When called up within a layout environment, it scans the circuit layout for inductive structures (spirals and interconnects). Each spiral or RF interconnect instance is then divided in segments, the absolute length of which depends on the operating frequency of the circuit. Each segment is modeled taking into account its series inductance and resistance, its parasitic capacitance to the underlying metal layer or the silicon substrate, the underlying substrate parasitic network and the coupling capacitances to the neighboring segments. The next step in the modeler's algorithm is the calculation of the mutual inductance values and coupling coefficients for the whole layout. With the segments already determined from the previous step, the modeler calculates an equivalent mutual inductance between every possible pair of segments in the layout, regardless of whether such segments belong to spirals or RF interconnects.

The modeling engine has been tested extensively against measured inductive devices on fabricated silicon. An array of spirals of various sizes has been measured in a 0.18um CMOS process. The measured data were compiled and compared against the results produced by the modeling engine and those produced by a commercial EM simulator based on the method-of-moments (MoM). These comparisons are shown in Figure 2 through Figure 5. As the figures show, prediction of low-frequency inductance (Ldc) and maximum quality factor (Qmax) is very good, while the modeling engine is noticeably more accurate than the MoM tool in the prediction of self-resonance frequency (SRF) and Qmax frequency.

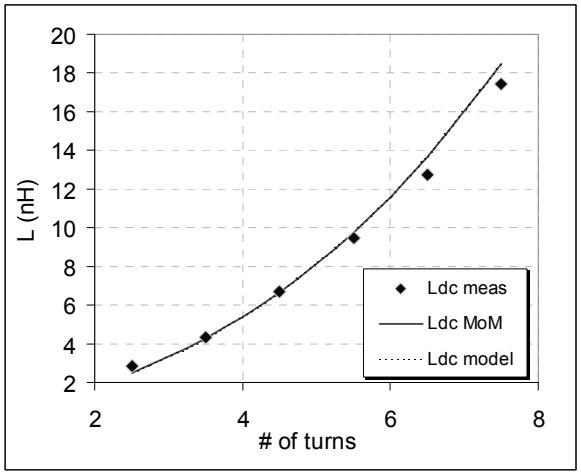


Figure 2. Low-frequency inductance comparison

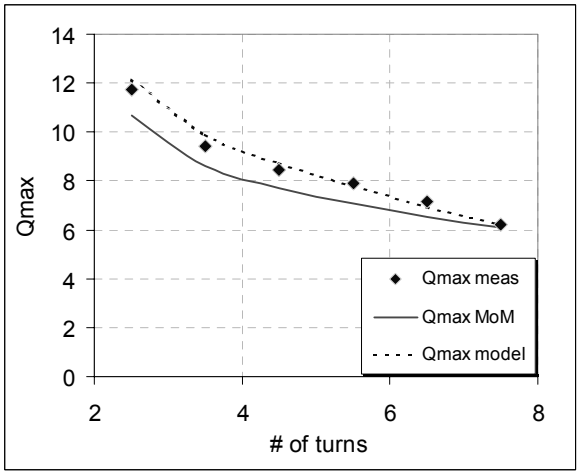


Figure 3. Maximum quality factor comparison

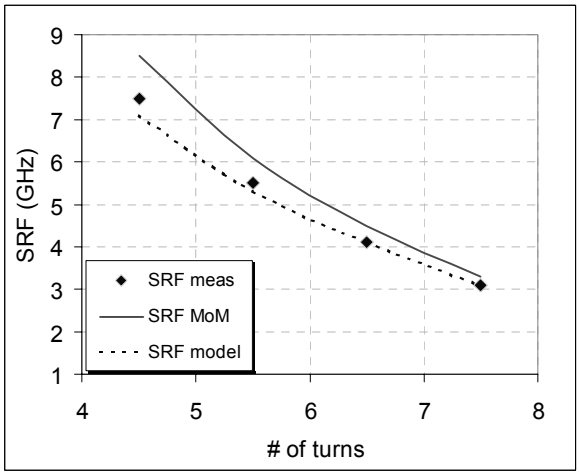


Figure 4. Self-resonance frequency comparison

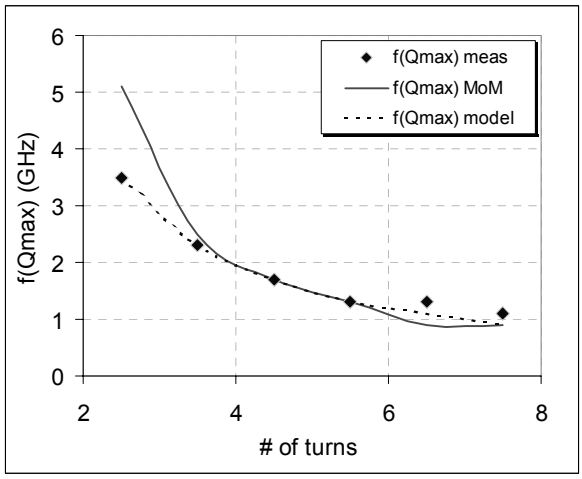


Figure 5. Qmax frequency comparison

3. Description of the proposed flow

A design interface is set up in the Cadence[1] IC design environment [2][3] using the SKILL language. The interface plugs in the Virtuoso toolset, and is seamlessly integrated with the Diva and Assura extractors.

Through a simple menu item added in the layout editor (Figure 6), the user can easily extract the models of simple spirals, interconnect lines, arbitrarily-shaped inductor structures or even complete circuits. A smooth handover between VeloceRF's modeling engine and RCX extraction engines enables whole layout extraction with all inductors taken into account.

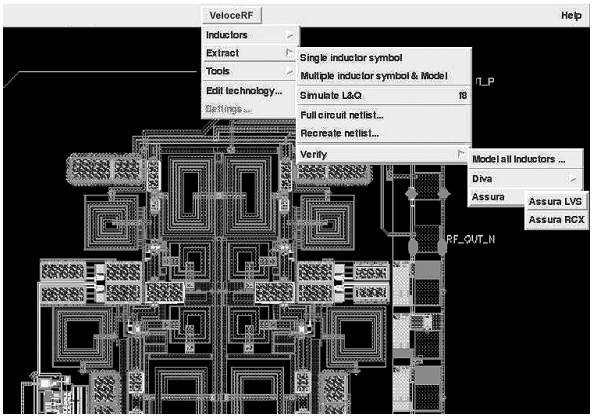


Figure 6. VeloceRF integrated in Virtuoso

Spiral inductor parametric cells (p-cells) are provided (Figure 7), that can be extracted with full connectivity in a unified extracted view along with other layout devices and parasitics.

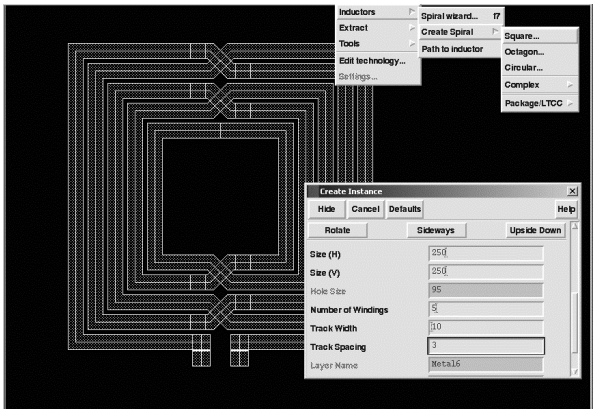


Figure 7. Differential inductor p-cell

Additionally, the flow can be combined with a substrate analysis tool, for achieving the first ever, true whole-chip RF IC modeling and simulation flow. The flow overcomes several shortcomings and furthermore allows an increased degree of design automation. Automation is enabled by a set of programming routines which perform the following processes in sequence: (a) Recognize the spiral inductor structures in an IC layout. (b) Associate the appropriate simulation model (i.e. netlist) with each inductor. (c) Generate a netlist containing mutual inductance and capacitance elements that model the topology-dependent coupling effects among all possible pairs of individual inductors in the layout. (d) Merge all the above netlists of individual inductor models and mutual inductance/capacitance elements into a unified netlist (netlist1), while appropriately assigning connectivity information (i.e. node names) between the disparate netlists. (e) Call up the extractor (e.g. Diva) which extracts layout information and recognizes transistor, resistor, capacitor, diode and parasitic devices from the layout and generates a new netlist of such elements (netlist2). (f) Merge netlist2 and netlist1 into a new netlist (netlist_sim), in an appropriate manner that assigns layout-correct connectivity information (i.e. node names) between netlist1 and netlist2. (g) Prepend the appropriate commands in the netlist_sim file so that it can be directly simulated by a SPICE-type simulator

3.1. Recognition of spiral inductors in the layout

To enable spiral recognition (as per step (a) above), each inductor in the layout is described by two extra (dummy) layers drawn at the tips of the inductor so as to 'cut' the single path that forms the inductor and create two terminals. In this fashion, a particular inductor model netlist can be considered being connected between the two terminals. Spiral inductor parametric cells are provided in VeloceRF, including all the necessary dummy layers plus the appropriate parameters to facilitate automatic layout generation of complex inductor structures. Apart from the modeling of p-cell spirals, the designer is free to form any kind of geometry and convert this geometry to an inductive element (inductor) by using a special procedure (path2inductor - Figure 8).

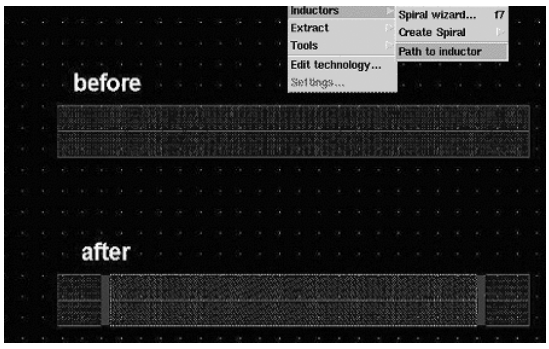


Figure 8. Converting a path to an 'inductor' cell

[1] Cadence®, Assura®, Diva® and SKILL® are registered trademarks of Cadence Design Systems, Inc.

3.2. Model extraction process

Inductor p-cell properties feed the modeling engine with all the necessary information, i.e. geometry and/or connectivity, and a netlist is extracted for each of the inductors. In addition, a netlist containing mutual inductance elements that model the topology-dependent coupling effects among all possible pairs of individual inductors in the layout is automatically generated. The above netlists of inductor models and mutual inductance/capacitance elements are merged into a unified netlist, while appropriately assigning connectivity information (i.e. node names) between the netlists.

Additionally, special SKILL routines in the flow assign to the p-cell's pins unique names that may be used as connecting points for the inductor netlist and the netlists created by other extractors and/or substrate analysis tools.

3.3. Interface with extraction tools

By adding some extra lines to the extraction deck, VeloceRF inductor p-cells are appropriately masked out of the extraction process, while connectivity annotation between the extractor's resulting netlist and VeloceRF models is handled as per paragraph 3.2 above. Additionally, a symbol that represents the final merged netlist is produced in the course of the flow. This can be placed in schematics and simulated in any simulator of choice.

In typical cases, the inductor-specific flow adds less than a minute to the time taken by the RC extractor. Assuming the designer just wants to trim the inductors on the final layout, the complete updated model can be recreated in less than a minute, bypassing a new extraction step. Table 1 displays the inductor extraction times of typical RF blocks such as LNAs, VCOs, PAs and mixers compared to the RC extraction times for these blocks. It is obvious that the total time overhead is minimal, making the proposed solution even more compelling.

Table 1. Inductor models extraction times in typical RF block cases

Type of RF block	Component count	Total spiral inductors	RCX extraction time	VeloceRF extraction time
LNA 5GHz	2921	12	8min 40sec	40sec
PA 2.5GHz	1963	14	2min 8sec	32sec
VCO 5GHz	326	4	10sec	4sec
I/Q modem	726	8	55sec	15sec

The flow is amenable to highly integrated RF IC design, particularly on silicon processes such as CMOS, BiCMOS, SiGe BiCMOS, SOI, MEMS, and to compound semiconductor processes (e.g. GaAs). It is also applicable to substrate technologies, such as LTCC and BT, where inductors and passive circuits comprising inductors can be designed.

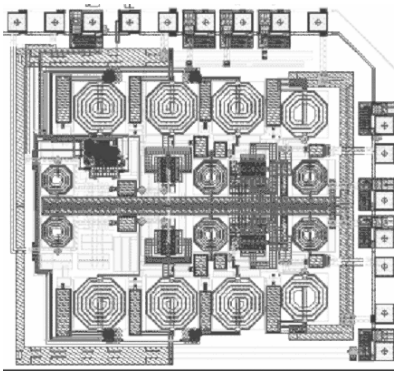
4. Real-life results

The proposed flow has been validated against experimental results of simple inductor structures and devices as well as complex RF blocks and transceiver designs. In this section the experimental results of a showcase power amplifier are presented, which was designed for 802.11b/g applications in SiGe BiCMOS.

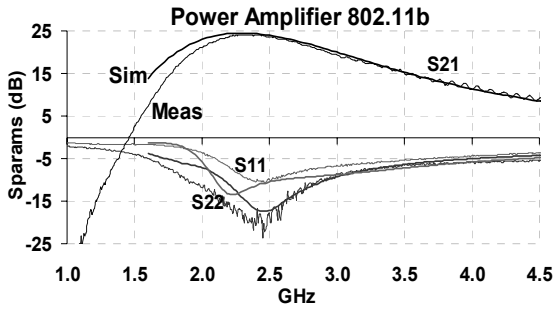
As mentioned above, most of the silicon foundries today provide simple inductor models from a pre-characterized library in their design kits. Due to the lack of mutual inductance models between spirals, as part of their DRC rules foundries enforce minimum distances between on-chip inductors, which results in significant silicon real estate loss. To exhibit the accuracy of the proposed flow and to emphasize the benefits, a very condensed layout design of the PA was generated using VeloceRF (Figure 9a). The layout intentionally violated the minimum spiral distance DRC rule provided by the silicon foundry. Thanks to the accurate self and mutual inductance modeling of all intentional and parasitic inductances, the power amplifier exhibited a very accurate measured performance compared to the simulated one, while the power output levels and its linearity proved to be adequate for the specification of the IEEE 802.11b/g WLAN (Figure 9b and c).

5. RF IP portability and re-use

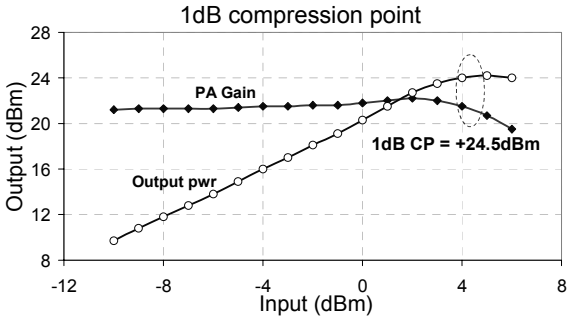
The proposed flow addresses a more efficient RF Intellectual Property (IP) portability environment (Figure 10). By enabling fast and efficient inductor modeling, the proposed technology covers a significant gap towards the whole-chip modeling of RF ICs. A good use of this capability is in the development of RF IP behavioral models. The performance of every RF block comprising spiral inductors is highly sensitive on the performance of the inductors themselves. In other words, if the inductor content of an RF IP block has been accurately modeled and characterized, then the overall behavior of the RF block may be easily defined, resulting in an accurately captured RF IP model. Captured models of RF IP can be easily evaluated, traded and used constructively in new designs, leading to first-pass silicon success. Co-integration of multiple RF blocks is also made easier, since RF coupling



(a)



(b)



(c)

Figure 9. (a) Layout of a balanced power amplifier for IEEE 802.11, (b) comparison of measured and simulated S-parameter results, and (c) power output and 1-dB compression point

effects are taken into account. Once the above have been achieved, portability becomes possible and legacy RF IP may be rapidly re-targeted.

A possible exploitation of the proposed flow is in the implementation of 'semi-hard' RF IP. With whole-chip models available through the flow, designers can rapidly customize and optimize the performance of an RF block by tweaking only the inductors and passives of the block. These capabilities go against the perceived oxymoron related to RF IP reuse and portability.

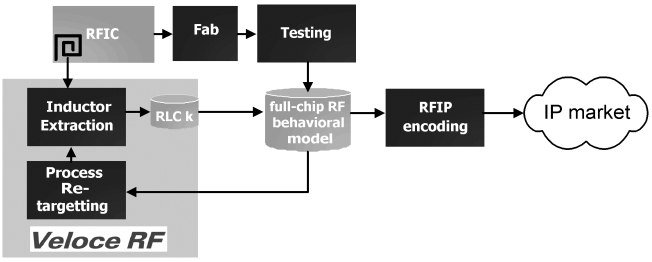


Figure 10. RF IP portability and trade flow

6. Conclusions

An efficient modeling flow and a novel modeling tool has been presented, addressing the accurate prediction of the performance of integrated inductive elements and RF blocks comprising inductors. The flow can be seamlessly integrated in a typical RF IC design chain, employing other tools such as a layout editor and RCX extractor. A design aid is established, for meeting demanding RF design requirements, while minimizing silicon real estate and development time. The flow can enable RF IP capture and re-use, overcoming many of the known barriers.

References

[1] Yorgos Koutsoyannopoulos and Yannis Papananos, "Systematic Analysis and Modeling of Integrated Inductors and Transformers in RF IC Design", *IEEE Trans. on Circuits and Systems II*, vol. 47, pp. 699 – 713, Aug. 2000.

[2] Cadence web site, www.cadence.com.

[3] S. Bantas, Y. Koutsoyannopoulos and A. Liapis, "Novel Inductance Modeling Flow Enables Whole-Chip RF Simulation," in Proc. International Cadence Usergroup Conference (ICU 2003), Sep. 2003.