A 16 Bit + Sign Monotonic Precise Current DAC for Sensor Applications

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Abstract

A 16 bit + sign monotonic precise current DAC for sensor applications working in a harsh environment is described. It is working in a wide temperature range with high output voltage swing and low current consumption.
The converter is based on current division and segmentation techniques to guarantee monotonicity. Two active cascoding loops and one follower loop are used to improve the output impedance, the accuracy and the voltage compliance of the DAC. The resolution of the DAC is further increased by applying PWM to one fine LSB current. To achieve low power consumption unused coarse current sources are switched off. Several second order technological effects influencing final performance and circuits dealing with them are discussed.

1. Introduction

Fast development of electronics in the last years with more and more advanced and precise sensors requires also more precise electronics to drive the sensors and measure their outputs. Some sensors only work in a very narrow operating window which must be externally controlled, e.g. a very narrow temperature range. They must be kept in their optimum operating point by applying very precise voltages or currents.

For such application we designed a current DAC. The main requirement for this DAC is 17 bit resolution (16 bit + sign bit) with guaranteed monotonicity and no missing codes. Another requirement is a linear output voltage range from 0.9 V to 3.8 V for a minimum supply voltage of 4.75 V. The absolute accuracy of the full DAC including the on-chip voltage reference is ±1.3 % over the full operating temperature range (-40 ^{O}C to 150 ^{O}C die temperature), excluding the external resistor for reference current generation. The current to the sensor must be continuous, which excludes the use of calibration cycles. There are no special requirements for settling time of the DAC.

2. Principles to achieve inherent monotonicity

The most demanding requirement is monotonicity and no missing codes over the full converter range, requiring a differential non-linearity (DNL) below 1 LSB.

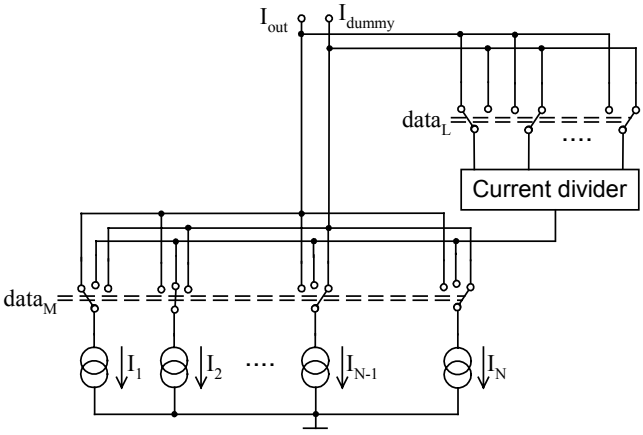

Fig. 1 Block diagram of segmented current dividing DAC

Fig. 1 shows a segmented current dividing DAC with inherent monotonicity [1], [3]. An array of identical coarse current sources $I_1 \ldots I_N$ is used. The coarse current sources I_1 to I_{Nc} are switched directly to the output I_{out}. The coarse current I_{Nc+1} is switched to the fine current divider. The remaining course current sources are switched to the dummy output I_{dummy}. The fine current

divider is usually binary weighted [1]. Coarse output currents and fine output currents are added and the total output current is

$$I_{out} = \sum_{i=1}^{Nc} I_i + I_{Nc+1} \sum_{i=1}^{Nf} k_i \,, \qquad (1)$$

where k_i is current dividing factor of fine current divider (sum of k_i of the full fine block is equal to 1)
Nc is number of selected coarse bits
Nf is number of selected fine bits.

The main advantage of this segmented current dividing DAC is its inherent monotonicity with respect to mismatches of coarse block current sources. The drawbacks of this configuration are the large area of the current source arrays for a 16 bit DAC, the limited output impedance without cascodes or the small output voltage range with cascodes on the current sources and the constant, high power consumption. These drawbacks are discussed in the following points.

2.1 PWM resolution enhancement

To decrease the number of current sources in the coarse and fine blocks and also to keep the value of 1 fine LSB current at a reasonable level, a pulse width modulation (PWM) is applied to 1 fine LSB current. This reduces the area of the current source arrays. To preserve the inherent monotonicity of the DAC, the fine current divider has to be linearly weighted and the PWM modulation has to be applied to the first fine output not continuously connected to I_{out}. The very small PWM output current is integrated on a capacitor or on the sensor itself.

The total output current consists of the coarse output current, the fine output current and the PWM modulated current.

$$I_{out} = \sum_{i=1}^{Nc} I_i + I_{Nc+1} \sum_{i=1}^{Nf} k_i + I_{Nc+1} k_{Nf+1} \frac{t_{PWM}}{T_{PWM}}, \qquad (2)$$

where t_{PWM} is the PWM pulse width and T_{PWM} is the PWM period.

2.2 Active cascoding of current sources

Contrary to a current DAC with a voltage output, the output voltage is not constant and the output impedance and voltage compliance become important. In our application the voltage headroom for the full DAC is in worst case only 0.9 V. To achieve high accuracy, high output impedance and low DNL, active cascodes on the coarse current sources and the fine block divider are required.

By adding OA2 (Fig. 2), the fine block is configured as an active cascode for the coarse block. OA1 and MC1 form a common active cascode on the coarse current source output. Finally OA3 buffers the voltage on the output pin N_{out} to node N_{dummy}. This makes the same drain voltage for all fine bit transistors and improves the current division accuracy without an extra cascode. Using active cascades, the coarse or fine bit transistors can be operated close to linear mode without accuracy and monotonicity degradation.

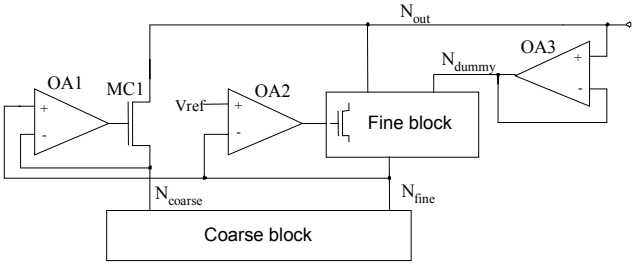

Fig. 2 Active cascoding structure

In Fig. 2, the positive input of OA1 is connected to N_{fine} instead of V_{ref}. In this way, the voltage difference between nodes N_{fine} and N_{coarse} is given only by the offset of operational amplifier OA1 and not by the combined offset of OA1 and OA2. Note, that the opposite connection is not possible because for currents below 1 coarse LSB, no current is flowing through the MC1 cascode and node N_{coarse} is floating.

During measurement of the DAC, it was found that for low temperatures impact ionization (hot electrons) in the cascoding transistor MC1 caused an error of several LSB when changing the output voltage ±1.3 V (even for long channel NMOS transistor). To solve this, a double cascode with two regulation loops was used – see Fig. 4, MC4 and OA4.

2.3 Decreasing power consumption

It is a well-known approach to achieve good linearity to dump the unused coarse current sources. When doing this the current consumption of the DAC is constant over the code. In our application the DAC is typically working with much lower currents than the maximum output current and low current consumption is important.

To save power, unused coarse current sources are switched-off instead of dumped in a dummy node. This significantly decreases the current consumption when the DAC operates at low output currents, but is known to be much less linear and requires a very careful analysis of all resistances in the coarse block current mirrors. Even small metalization resistances can significantly influence the absolute accuracy and the DNL of the converter due to changes in the current pattern for successive switching of the coarse current sources. The source side of the current sources is of course very sensitive but also the node N_{coarse} is important since the transistors work close to linear

mode. A full backannotation after layout of all resistors in the array has been done and the converter accuracy and DNL have been verified.

In order to limit the series resistances, all mirror transistors inside the coarse blocks are mostly covered by metal. Excessive metal coverage over matched transistors can cause V_t shift [5] and significantly degrade matching. To solve this, a special annealing process step was added in the processing.

3. Complete schematic

Fig. 3 shows how the 17-bit digital input word is split between coarse, fine and PWM blocks.

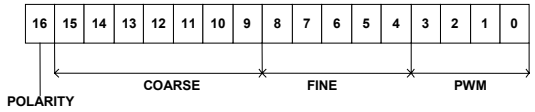

Fig. 3 Separation between coarse block, fine block, and PWM block

To realize the sign (polarity) two 16-bit current DACs are constructed, one with NMOS current mirrors sinking current and the other one with PMOS current mirrors sourcing current.

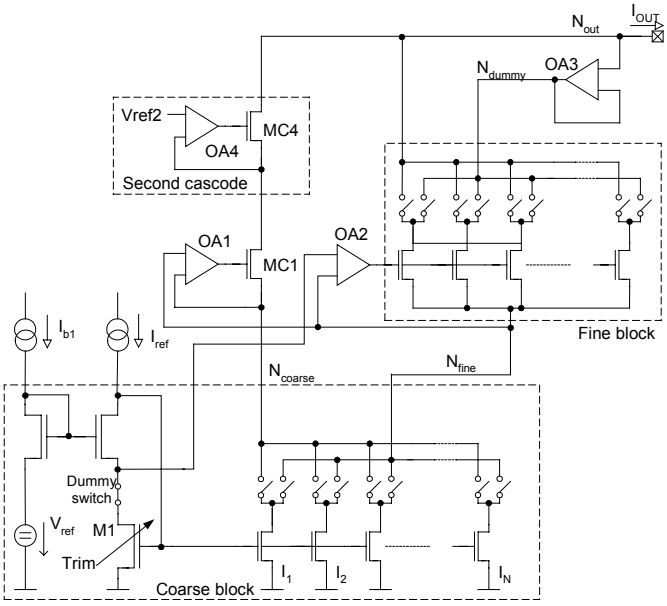

Fig. 4 Block diagram of the NMOS current DAC

The complete block diagram of the NMOS current DAC is shown in Fig. 4. The coarse block is a linearly weighted low drop current mirror. The outputs of the $I_1 \ldots I_{Nc}$ coarse currents are fed to the cascode MC1. The I_{Nc+1} coarse current is connected to the fine block where the current is further divided. The remaining coarse currents are switched-off. On the outputs of each coarse current source, two switches are used. The first switch is controlled by a thermometer code and the second switch is controlled by a code 1 of N. The fine block is also a linearly weighted array and PWM is applied to the first fine output not connected to N_{out}. On the outputs of each fine current source, two-way switches are used, which connect the currents to output N_{out} or to the dummy branch N_{dummy}. The first switch not continuously connected to N_{out} is modulated by the PWM signal.

In Fig. 4, the active cascode loops and the dummy node buffer are also shown. The reference current branch contains a dummy switch to compensate the voltage drop on the switches of the coarse block.

The current offset of the PMOS and the NMOS current DACs is trimmed by adjusting the W/L ratio of reference transistor M1 and the optimum trimming code is stored in a one time programmable memory. To find the optimum trimming code and limit the trimming time, only the coarse currents are measured. (Fig. 5).

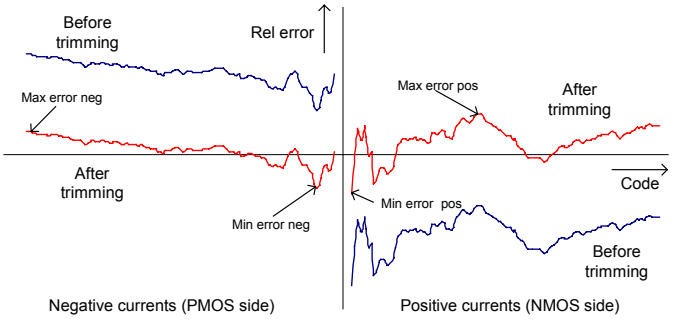

Fig. 5 Trimming of absolute accuracy

4. Detailed construction of the matrices

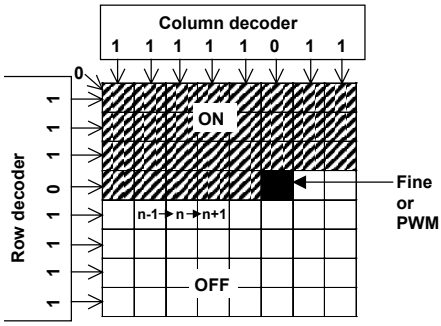

Fig. 6 Realization of decoding

Both coarse and fine blocks are constructed in a matrix structure. Each matrix cell contains the mirror transistor, the two current switches and a logic circuit, which combines the row and column decoder inputs with the status of the previous cell to control the current switches. This embedded logic control decreases the matrix layout and decoder complexity but it lowers the large signal response of the DAC due to its serial structure. The speed

of the DAC was not an important requirement of the system. Fig. 6 shows a simple arrangement for a 6-bit matrix with the row and column decoder signals and the serial input signal for the first cell.

The structure in Fig. 6 is vulnerable to processing gradients. Better linearity is achieved by randomization of the decoders at the expense of more complex layout. A good compromise between complexity and accuracy is obtained by the pseudo-random organization in Fig. 7, where also the four trimmable reference transistors M1a…M1d are shown.

Column decoder switching sequence

Row decoder switching sequence										
	5	6	7	8	1	2	3	4		
7	M1a	53	54	55	56	49	50	51	52	M1c
5		37	38	39	40	33	34	35	36	
3		21	22	23	24	17	18	19	20	
1		5	6	7	8	1	2	3	4	
2		13	14	15	16	9	10	11	12	
4		29	30	31	32	25	26	27	28	
6		45	46	47	48	41	42	43	44	
8	M1b	61	62	63	64	57	58	59	60	M1d

Fig. 7 Pseudo-random switching sequence of a 8 x 8 matrix

The embedded logic for the NMOS coarse matrix is shown in Fig. 8. The row and column decoders are 1 of N decoders with negative logic output (negative logic simplifies the embedded logic). Signal Nminus1 is the output of the previous cell and is set to zero for the first cell. It propagates a zero and closes switch SWOUT through the matrix until the selected cell is reached. For the selected cell the signal SWFINE is one, SWOUT is zero and Nplus1 is one. This current source is connected to the node N_{fine}. For all following cells Nminus1 is one, and the current sources are switched off.

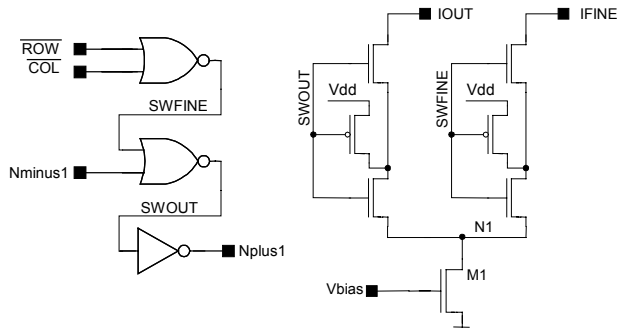

Fig. 8 Coarse block cell including decoder, current source M1 and switches

During measurement it was found, that the NMOS side DNL error increased at high temperatures. This error was caused by off-state channel leakage through the coarse block switches. At 150 ^{O}C the channel leakage increased to 1 nA per switch, causing several LSB DNL error at coarse bit changes for low currents. This was solved by using double switches with middle point connection to the supply – see Fig. 8.

The embedded logic for the fine block is shown in Fig. 9. This logic includes a multiplexer, which connects SWOUT to the switches before the selected cell and connects the PWM signal to the switches for the selected cell only. Complementary switches are used to cancel clock feed through.

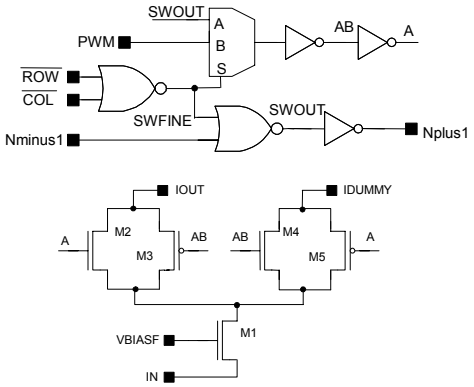

Fig. 9 Fine block cell including decoder, current dividing transistor (M1) and complementary switches

5. Realization and measurements

The DAC was processed in a 0.7 µm, n-well CMOS technology with single polysilicon and double metal interconnect. Layout area of the DAC is 1.4 mm^2. The die photo showing the DAC with different blocks is in Fig. 10. The maximum output current is ±6.5 mA and 1 LSB corresponds to a current of 99.2 nA.

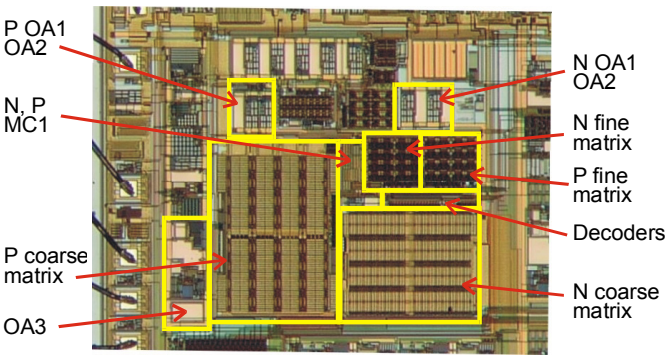

Fig. 10 Photo of the realized 17 bit DAC

Fig. 11 shows measurement results of DNL at coarse bit changes (where the DNL error is maximum). The residual error is mainly caused by metal resistance of ground and supply tracks. Absolute accuracy over temperature is shown in Fig. 12. The larger temperature

variation for positive currents (NMOS side) is caused by residual V_t shift due to not perfect annealing. An updated version of the converter with decreased metal coverage and improved annealing process is in processing.

Worst case settling time of the DAC happens when the polarity of the current is reversed, it means one part of the DAC is almost switched off to save current consumption and the other part is starting to operate. When switching to maximum output current we need also to charge the biggest capacity on the gates of the coarse block mirror transistors. Measurement results of such a worst case settling time when switching between code –65535 and 65535 is shown in Fig. 13. Measured settling time when switching polarity for maximum current to achieve full accuracy is below 20 µs.

Finally, on some samples an accuracy shift at low temperatures (0 ^{O}C to -40 ^{O}C) is observed. This is caused by package stress, which increases at low temperatures and depends on the package type. Because of this, the DAC is trimmed at low temperatures.

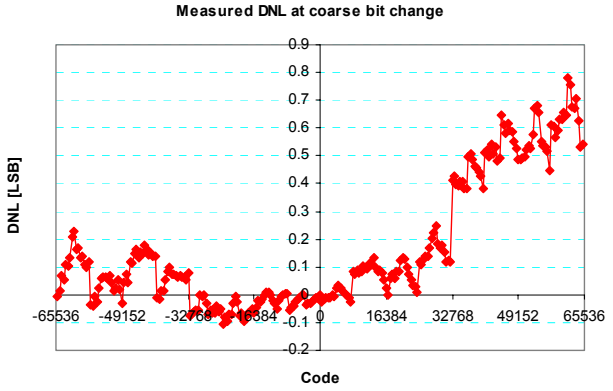

Fig. 11 Measured DNL error

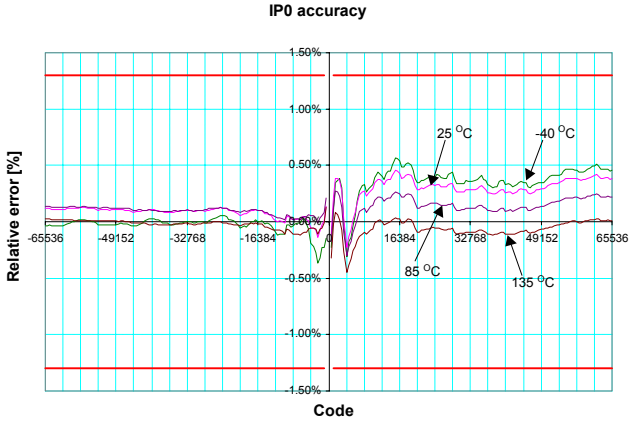

Fig. 12 Measured absolute accuracy

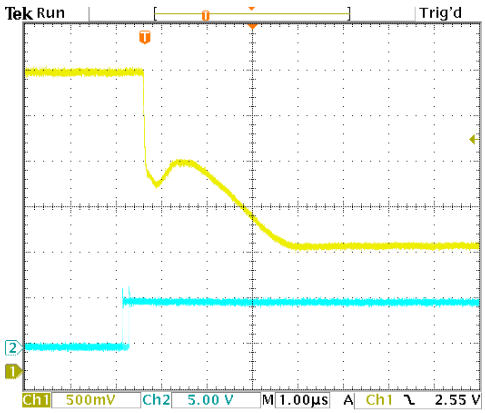

Fig. 13 Measured settling time (channel 1, output is connected to 150 Ω resistor at 2.35 V)

6. Conclusions

A low power consumption 16-bit + sign monotonic precise DAC with current output was realized in a single poly 0.7 µm CMOS process. It uses a 7-bit coarse current source, a 5-bit fine current divider and a 4-bit PWM. Using this segmentation technique, linearly weighted blocks and active cascoding, monotonicity over the full converter output voltage and temperature range was achieved in a small area.

Higher order effects like metalization resistance, impact ionization, off-state channel leakage, V_t shift due to metal coverage and package stress at cold were discussed and solutions were shown.

Acknowledgement

The author would like to thank Dr. H. Casier for his very valuable comments to this paper and great support.

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