Highly Digital, Low-Cost Design of Statistic Signal Acquisition in SoCs

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Abstract

Presently, the gap between analog and digital processes is ever increasing. Although digital circuits are still obeying Moore´s law, their analog counterparts follow far behind. Since signal acquisition, through ADC circuits is an often required feature, for many embedded applications the benefits of Moore´s law have not been achieved. This paper presents our approach to take advantage of the increasing integration of technology for analog interfacing in SoC's, by converting the statistics of the signal. Digital self-tuning of the threshold levels, the use of less expensive and highly variable analog blocks, and stochastic convergence of resolution allow a robust acquisition process. We present the mathematics behind the approach, as well as a set of target applications and experimental results validating the concept.

1 Introduction

As fabrication technologies progress further into deep-submicron scales, the average digital processing power available for applications design increases exponentially. This leads to potentially smaller and cheaper devices, which usually means a wider range of viable SoC (System-on-Chip) applications. Since many of these need to acquire data from the physical world or to communicate through a variety of physical media, analog interfacing is often required. ADCs are expensive to integrate since they are very dependent upon component accuracy [1] whereas digital technologies have a higher yield than analog ones. Also new digital deep-submicron processes offer even higher variability in their electrical and geometrical properties than previous ones, meaning that the existent analog-to-digital gap is not about to narrow. Follows that an ideal conversion process would be mainly digital or enabled to use less demanding analog parts by a more sophisticated digital signal processing.

For highly integrated digital systems with fewer visible internal blocks, wider process variations drive higher amounts of the production cost to be allocated in the testing phase. Strategy to minimize this problem has been twofold: increase design automation and verification to minimize project mistakes; and provide on-chip test facilities either as Design for Testability – DfT; or Built-In Self Test – BIST[2]. ADC design automation face a granularity problem, since it must compromise with a given set of architectures and process dependent analog modules [3][4]. Moreover, to include built-in self-test an additional highly reliable analog reference generator must be provided [5].

There's also a specification issue to deal: traditionally, everyone using ADCs tries to reconstruct the analog signal. Using this approach, the resolution of the converter (number of bits) plays a major role. However, for many SOC applications, the digital data the system actually needs is not a full reconstruction of the input signal, but rather a measurement that can express some statistical properties of it, and may be less hardware demanding. Analog self-test [6,7,8], passive sensors signal conditioning [9], low-frequency data acquisition [10-12](where high over-sampling ratios can be used) and the many designs that employ adaptive modeling and stochastic grouping algorithms are instances where one may profit from application specific designed acquisition.

To propose a low cost, easily automated methodology to analog interfacing on mainly digital SoCs we focused on statistics acquisition rather than signal reconstruction. Main features are: (i) the basic block is a extremely low-cost 1-bit stochastic sampler; (ii) from the bottom-up perspective architecture allows components with high variability and non-ideal behavior (e.g. high offset comparators); (iii) from the top-down perspective, acquisition can be fine-tuned for specific applications; (iv) parallelism, redundancy, self-configuration and active dithering are used to transfer design complexity to the digital domain; (v) built-in self test is a embedded feature; (vi) it is an over-sampling technique, a desirable feature given the ever increasing switching speeds of transistors.

This work shares some features with other recent lines of research, section two reviews the main contact points, explain differences and hopefully clarifies the proposal. Theoretical background and acquisition structure is presented in section three. An experimental setup was designed to validate the concept and its measurements are the subject of section four. Section five presents discussion of results and future developments.

2 Related Works

In recent research some groups have also pointed-out to the potential advantages of both application specific

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ADC design and over-sampled acquisition for SoC's. The most widely used architecture in this line of research is based on ΣΔADCs (e.g. see [4]). Our proposal, while also stresses over-sampling, does not rely on noise-shaping. Thus, stochastic sampling have slower convergence, but also can use smaller, more variable, analog blocks. The bet is that in the long term, gains in parallelism will pay. Also, within the stochastic acquisition framework, there is no reason one should not try to use feedback to control noise generator statistics and improve convergence in a specific application. It would undoubtedly be a hard non-linear control problem, but nevertheless a digital one.

In low-frequency instrumentation there is already well established research relying in statistic acquisition. In a sense, stochastic sampling shares many similarities. Main differences is our focus in the acquisition of statistics as an application-driven feature, and that much of this previous work uses some kind of well-behaved repetitive reference instead of noise[12]. Modern signature based proposals for analog test [6-7] use a similar approach. Using noise has the advantage of potentially easier and more robust hardware design, and producing a more well-behaved uncorrelated quantisation error. This later feature allows for pattern-identification applications at higher frequencies [13]. A similar emphasis on the acquisition of statistics is found on the work of Tapang and Saloma [11], however they also use a sinusoidal reference in a combination of zero-crossing and noise dithering.

A rather recent work [14] proposed a adaptive strategy to reduce the area cost of comparators on flash ADCs. It was able to show that using redundancy of highly variable circuits one can achieve a better area usage. Statistic sampling similarly relies on parallelism of simple blocks, but goes further using more robust noise references and a clustering model to deal with threshold scattering.

3. Theoretical background

3.1. Statistics Acquisition

Analog to digital conversion is a tradeoff between parallel comparison with fixed threshold levels and serial comparison with a time varying reference. Quantisation theory [15] provides a mathematical framework to digital acquisition. For any well known input signal, a family of additive references can be defined that leads to a optimal relation between resolution and convergence [16]. ΣΔADCs are the most common way of trading statistic knowledge about the signal behavior and acquisition performance. Higher order noise-shaping convergence depends upon signal characteristics and can be likened to a non-linear control problem [17]. In this context noise dithering is often employed as means to force quantisation error to be distributed in the spectrum [18-20].

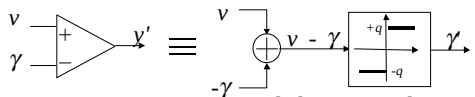

Figure 1. Comparator model as a subtractor plus a hard-limiter.

Figure 1 shows the model of a single comparator: analog signals are added, then area sampled by a hard-limiter. Also, one sees (Figure 2) how the probability distribution function (PDF) of a constant value and a uniform random noise are combined. From a given PDF one can calculate signal first-order statistics. As two signals are summed in the time domain, their PDFs are convoluted.

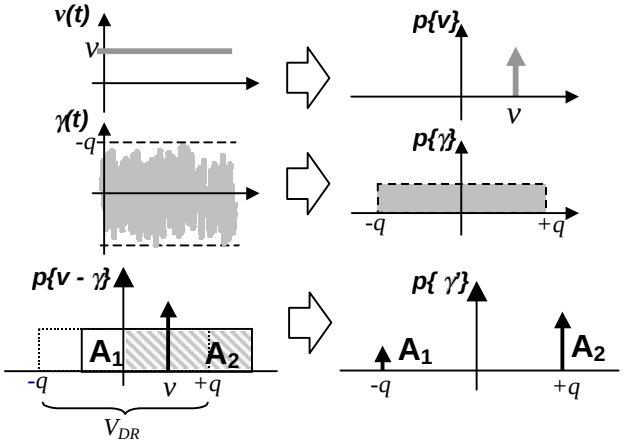

Figure 2: Acquisition with dithering. Signal (*v* – a constant value) and noise (-*γ*) PDF's are convoluted and area sampled by the 1-bit AD. Statistics before and after quantization are related, and the resulting bit-stream (*γ'*) can be used to infer properties *v*.

The resulting distribution is then area sampled and gives distinct probabilities for the quantised signal. It's possible to use a similar approach to establish the relation between the self-correlation of the sampled pulse train and the input[19,20]. Applied to a hard-limited signal with gaussian distribution (γ) results in the so called arc-tangent relation (1)[21], used on some PSD based analog test methodologies [13].

(1) $R_{xx}\{\gamma'\} = (1/\pi) \cdot \tan^{-1}[\, R_{xx}\{\gamma\}/R_{yy}\{\gamma(t=0)\}\,]$

It's a know result from audio electronic that with a carefully chosen dither distribution one can establish a linear relation between an arbitrary power of the first order statistics of the analog signal and the same power the statistics of the quantised one [20]. Since digital processing the signal is not a issue we are not so concerned with the linearity of the relation. Therefore, equation (2) can be used to provide a reliable function (Γ)

linking the averages [19] of any signal $\boldsymbol{v}$ and the acquired bit-stream γ' for any known noise distribution.

$$(2)\quad E\{\gamma'\} = q \cdot \left[\int_0^{\infty} \left(p\{v\} \otimes p\{-\gamma\} \right) \cdot d\Omega \right]$$

This last relation will be used to reconstruct the statistics of the over-sampled analog signal from the estimated statistics of the acquired pulse train.

3.2. Stochastic convergence

Naturally, one cannot measure directly any signal statistics but rather infer its value using an estimator. Using the average estimator (3) one expects to have a estimates error probability that will be itself a stochastic variable related to *N*. From the Central limit Theorem [22], one should expect a gaussian error distribution for any meaningful value of *N*.

$$(3)\quad m(v, N) = \frac{1}{N} \sum_{i=1}^{N} v(t_i)$$

Since the error will have a flat spectral characteristic, a highly over-sampled signal will converge to its punctual value by reducing the total error power. Therefore, resolution can be re-stated as probable resolution in equation (4) where the worst case convergence is related to the number of estimates *N* taken.

$$(4)\ N = \left(P_O \sigma_\gamma\right)^2 \times 2^{2 \cdot r} = k_p \times 2^{2 \cdot r},\ where: k_p = \left(P_O \sigma_\gamma\right)^2$$

The factor P_o defines the likelihood of a estimate under the defined constraints. This property allows a framework where graceful performance degradation is a built-in design feature. A similar reasoning using PSD estimation can be applied, to well-known narrow band periodic signals as in passive sensor conditioning [9].

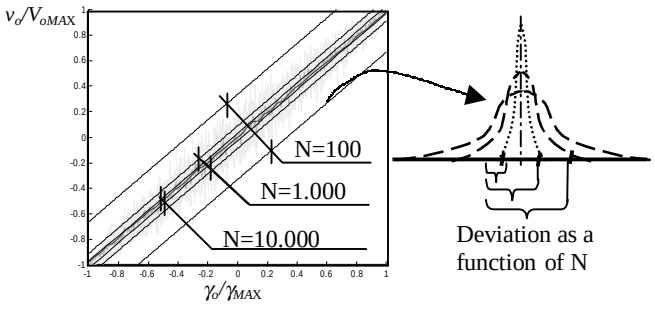

Figure 3. As averaging depth N increases, error scattering diminishes allowing higher resolution estimates.

Figure 3 displays a computer simulation of signal acquisition through stochastic sampling using a uniform noise reference. Output value is calculated through averaging the train pulse and applying reconstruction function Γ.

For non uniform dither distributions Γ is a non linear mapping and that may impact on resolution convergence. For instance, using a gaussian dither, Γ is a $\boldsymbol{erf^{-1}}$ function that is asymptotic near ±1 (Figure 4).

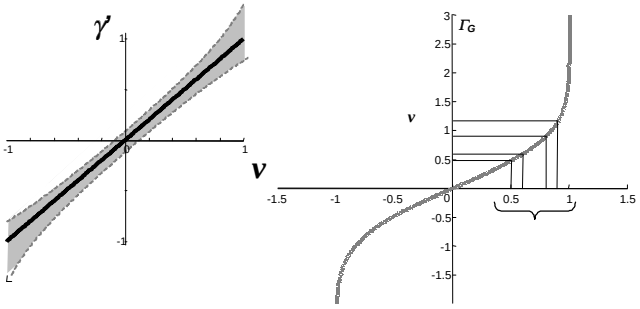

Figure 4. Non linear noise reference distribution (Gaussian) influence on resolution convergence. For a fixed value of *N*, resolution decreases a the *DR* fringes.

A higher gain in the periphery of the DR (Dynamic Range) means that one needs more estimates (*N*) to guarantee the same dispersion of the output. For fixed values of *N* that means that an stochastically sampled signal $\boldsymbol{v}$ will have a variable resolution with a peak next to the central values of the noise distribution ($\boldsymbol{E\{\gamma\}}$). This issue can be dealt with by using a noise amplitude greater than the *DR* of the signal to acquire [9].

3.3. Parallelism and resolution

Equation 4 dictates how one can trade resolution by bandwidth. As statistics estimation is a low pass process, with logarithmic convergence, higher resolutions demand really high over-sampling ratios $\boldsymbol{o_r}$ (5). But it is also possible to see another way to increase resolution: one can use a higher number of comparators, also zero-centered but using uncorrelated noise references, and combine their results. It is thus possible to take advantage of hardware parallelism.

$$(5)\quad o_r = \frac{1}{\left[k_p \times 2^{2 \cdot r + 1}\right]} \quad \text{, where } \boldsymbol{o_r = F_s / F_{MAX.}}$$

On a worst case estimate, if β comparators are used together with *N* statistic averages for each comparator, resolution will be give by *r* (6).

$$(6)\ \boldsymbol{r(v) = \tfrac{1}{2} \cdot G_\Gamma(v) \cdot \log_2 [(\beta \cdot N)/k_p]}$$

Where $\boldsymbol{G_\Gamma(v)}$ is a factor that mirrors the resolution variation in the dynamic range, as it influences non-linearity in reconstruction function. For acquisition with

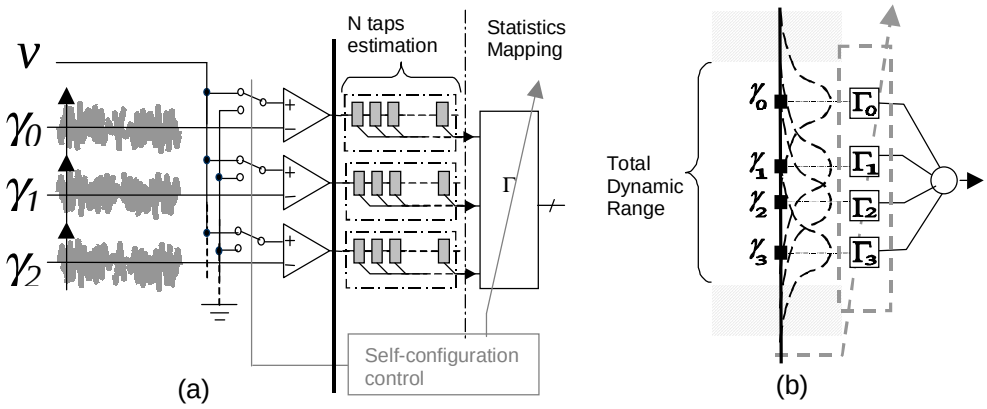

Figure 5: Acquisition architecture relies heavily on digital processing and self configuration using highly variable analog elements (a). Statistics estimation uses multiple noise references with overlapping regions of influence (b). This way analog offset variation expands the dynamic range (DR).

uniform noise G_Γ is unitary. Using gaussian noise this factor will have a big influence and may be mandatory in the *DR* fringes. Redundancy, self-configuration and a weighting mechanism provides the means to reduce this influence by taking advantage of the scattering of the reference distribution centers due to hardware variation.

3.4. Hardware variation

In the context of statistics acquisition only two types of analog blocks are required: noise reference generators and one-bit comparators. To allow a low area cost, one should use highly variable blocks. For comparators, this means randomly distributed offsets. For noise references this means we cannot assure a perfect zero mean distribution.

To deal with this scenario, the proposed architecture is adaptive. Digitally controlled switches can ground the signal input at a self-configuration stage. Once reference statistics are modeled the acquisition proceed. The complete architectures is show in Figure 5a. This setup provides two interesting characteristics: allow the use of less expensive comparators and provides a framework with embedded self-test capabilities.

Statistic reconstruction follow the model given in Figure 5b. Since offset varies, each noise generator can feed more than one comparator in a redundant circuit. Due to the scattering of the centers, once the references are modeled and the inputs are weighted one can reconstruct signal statistics using equation (7). If a clustering technique is them applied new center can be defined and the total dynamic range can be further expanded into the gaussian distribution fringes.

$$(7) \qquad \gamma' \cong \frac{2 \cdot DR_v}{DR_\gamma} \times \left[\frac{\sum \mu\{\gamma_n\} \cdot (\Gamma_n - \mu\{\gamma_n\})}{\sum \mu\{\gamma_n\}} \right]$$

Several uncorrelated noise sources can be provided in three ways: (i) using digitally sampled analog generators as the one proposed in [23] with different seeds; (ii) operating over other noise sources in the analog domain (e.g. using analog inverters); and (iii) delaying the original noise output through sample and hold.

To test the concept a straightforward averaging process was employed to self-configuration. Despite the simplicity the results are promising and an optimal configuration algorithm is still an open issue for research.

In the following section a series of measurements are performed in order to validate the proposed approach for signal acquisition.

4. Experimental Results

A prototype board was setup with four off-the-shelf LM311 comparators. Two HP3120 signal generators produced gaussian noise references. To generate four uncorrelated sources two analog inverter circuits where used. References where also low-pass filtered (@ ~10^5Hz) to cope with LM311 band restrictions. Data was acquired using a digital osciloscope (HP54645D).

Analog circuits where not fine-tuned, any correction should be performed in the digital domain. Before any acquisition, inputs where grounded and the digital data acquired to provide statistics estimation algorithm with a self-configuration stage. Statistics estimation assumed a single center combining all the inputs.

Two kinds of test where then performed: static tests, where a low frequency triangular signal where applied, and dynamic tests with sinusoidal inputs. A Tektroniks CFG 353, provided the inputs. Figure 6 shows a screenshot ; one of the four reference noise signals is also featured with a full scale sinusoidal input.

From the first set of measures the maximum resolution, IO characteristic, and the resolution variation with N, β and maximum dynamic range were verified.

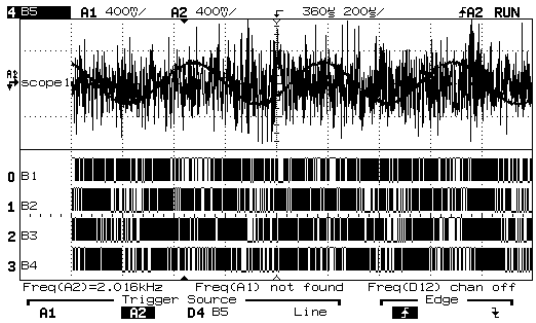

Figure 6. Acquisition screenshot, one sees DR restriction of the input. Only the digital channels are used in the acquisition algorithm.

4.1. Static features

Using a triangular signal with amplitude A = 2.1875V, offset VQ = 0.25V, and frequency f =24.9 (ou 249) Hz. Data was sampled with a frequency of Fs = 5Msamples/s. Noise references were set to have 6V around 3σ. Figure 7 shows the input/output characteristic of the process.

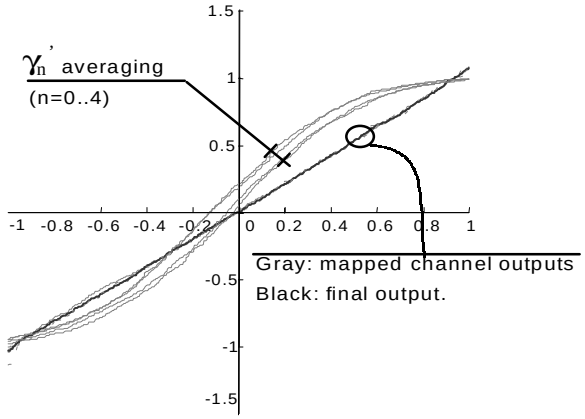

Figure 7. Outputs from averaging in each comparator and after non-linear statistics mapping.

Final output is calculated using equation 7 and the outputs of the four comparators. Since we have a stochastic convergence, estimating the resolution from the error will result in a distribution.

Figure 8, shows the distribution for different number of averages (*N*) and distinct degree of parallelism (*β*). The marked spots show that we can achieve a 8 bits resolution either using two comparators and N=20000, or using 10.000 averages and four comparators.

In Figure 8b is possible to see how the designer can exchange parallel comparators for additional averaging cycles. A continuum design-space using only low cost blocks is thus made available.

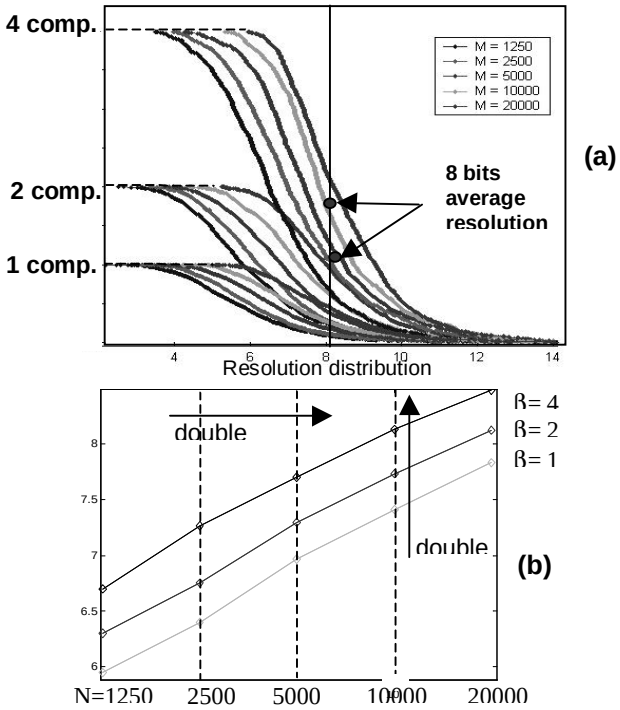

Figure 8. Parallelism and resolution. Equation 6 predicts min. resolution for a given pair (N,β)

On stochastic sampling, resolution also is a function is worst at the noise fringes. Figure 9 shows how the combined output reflects this characteristic. On the bottom of the figure the γ_n references are indicated.

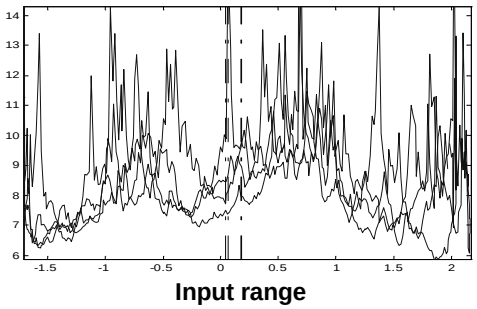

Figure 9. Resolution as a function of deviation from noise references centers. Dashed line shows the actual centers for γ_n.

5. Final Remarks and Future Work

This work puts forward the concept of direct highly digital, statistics acquisition. Measured results verified the theoretical data. However, these are only the first results, and there are still a number of open issues.

In future works we would like to:

(i) to determinate an optimal algorithm for the configuration stage of the architecture, ideally one should use noise sources with distinct variations and ranges;

(ii) use more sophisticated adaptive modeling to statistics reconstruction;

(iii) establish the minimal features and ideal architecture for the noise generator block;

(iv) define a automatic path from a higher level description of the application to the smaller statistics acquisition hardware.

Some of these results have already been achieved. A digital full prototype of the converter was designed and the costs evaluated. Table I shows the results.

SS-ADC			
DIGITAL BLOCKS (GATE COUNT)			
For 5 bits $N \cdot \beta = 2^{14}$	β =1	β =2	β =4
Averaging and weighting the acquired bitstream	2153	2250	2444
Random sampling generation*	764		
ANALOG BLOCKS AREA (μM^2)			
Generator Reference	27.474		
Comparator area	1.325	2.650	5.300

Table 1. Statistics acquisition cost

Next we intend to test the approach using digital specific digital process information. We also want to determinate the implementation cost of a prototype and compare results with other mainly digital low-area signal acquisition designs.

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