IP Testing – The Future Differentiator?

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Introduction

As more and more players come into the IP market and IP becomes more and more "commoditized", providers will need to identify other differentiators besides functionality and performance (ie. all providers will provide similar functionality and performance and may need to find another differentiator or be forced to differentiate on price). Test may prove to be a key differentiator for IP as testing challenges increase at the chip, board and system level and the call for quality becomes louder and louder. However, Design For Test will require a great deal more thought in an SoC flow with evolving technology.

Key Test Requirements for Soc

Advancing technology is creating a new, different defect spectrum. Current test techniques may be impractical for finding defects in newer technologies. As technology advances much more emphasis will need to be placed on "at-speed" testing over "static", stuck-at testing. At a die level, at speed testing may be difficult. Once the die is placed on chip the problem of at-speed testing (as well as any type of testing) becomes compounded by lack of access due to surrounding logic. Building at-speed test capability into the IP and providing capability to access that logic will be imperative to ensuring high quality both at the wafer level and after it has been integrated on to the chip.

Perhaps even more important will be the testing of external interfaces. Given the complexity and timing requirements of these interfaces, in addition to crosstalk and signal integrity effects which may occur due to the speed and density of the interconnects, testing "from the inside-out" will become more and more prevalent in the future. We can already see this to some extent with memory interfaces. Test capability is being built into the memory controller, not only to test the memory interface, but also the memory itself – all at speed. Without this built-in capability, memory testing would be virtually impossible in cases where the memory interface was not accessible at the chip level.

High speed SerDes is another example where "inside – out" testing can be effective. Building Bit Error Rate Test (BERT) capability and jitter test capability into the SerDes logic may reduce the requirement for very expensive equipment to test these parameters. Providing loopback capability in conjunction with built in BERT and jitter test will ensure an effective, at-speed test of the interface, whether or not there is access at the chip I/O.

Testing of processors and mixed signal IP will require a large number of functional vectors in order to assure high coverage. Built-in test features (functional BIST) will certainly help to reduce the vector count and increase coverage. Once again, given the complexity of the external interfaces of these IP, built-in, inside-out test capability would be very beneficial. The IP designer may again need to consider that external interfaces at the IP level may not be accessible at the chip I/O. Therefore, consideration has to be taken to make sure that built-in logic can be accessed and that any "external" requirements are specified so that providers of IP at the other end of the interface will know what test capability is required in their interface logic. In this case, it may not be as easy to specify and/or standardize external interface test requirements as it was with memory and SerDes logic.

Finally, as test capability expands beyond the borders of the IP, diagnostic capability also becomes important. Isolating to the offending logic is important for both cost and continuous improvement. It's easy to see that both test and diagnosis in the SoC environment will require careful consideration by the IP integrator. For diagnosis, inside-out and outside-in testing become equally important. "State cells" can be integrated into the IP to provide further isolation during functional testing of the integrated chip. Control of clock domains is also important for isolation of failing IP. Built-in test capability will be critical to achieving effective test and diagnostic capability.

Important Considerations

Assuming that the test logic which is described above can be implemented, at least 3 major considerations must be taken into account to guarantee that the "integrated" part can be effectively tested.

Power is a very important consideration for traditional ASIC's as well as SoC. More specifically, power requirements for testing can be significantly larger than power requirements for functional operation. It is important that IP providers specify test power requirements, and provide the capability to "quiesce" test logic while other IP is being tested. It is also important

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that the IP integrator work closely with the IP provider to guarantee that the effects of "quiescing" test capability will not be to minimize test coverage (either internally or externally). These considerations may also play an important role in determining IDDQ test capability. IDDQ testing is currently used to help identify and correct process related issues.

Effective test resource sharing is also extremely important in SoC test due to the complexities described above. This includes tester memory distribution, tester time sharing, tester IO access sharing and parallelization, (clock channels, scan chain, P1500 wrapper chain accesses from tester bus, etc). To achieve the highest overall test quality of the SoC with limited tester memory and time, tester memory and time should be distributed among IPs and core logic parts. The distribution should take into account the IP complexity and its defect density on the die. Logic implemented in the high defect density area should be thoroughly tested. Test access of IPs and core logic parts should allow for the maximization of parallel access and test within the allowed power budget. Built-in test logic helps reduce the amount of limited tester resources required and should be used as much as possible.

A final consideration comes into play if there are multiple IP with the same functionality. The test control logic and access should be shared among identical IPs as much as possible to save die area. The sharing should be flexible enough to allow both parallel test and individual serialized IP test for both volume production test and diagnosis purposes. Redundancy of IPs for repair should also be considered when the number of identical parts exceeds a certain limit. For example, redundant processors for massive processor array design.

If it is possible/preferable to interchange IP based on function and performance, it is very important that test access be identical in order to prevent the possible requirement of several test programs, based on different combinations of IP which are functionally equivalent but have different test access protocols. In cases which several instances of the same IP are integrated on chip, the requirement for different test programs could be in the 10's to 100's for an equivalent functional part.

Conclusion

Testing in an SoC environment requires careful planning on the part of the IP integrator, and careful attention to DFT on the part of the IP provider. DFT must be "outward looking" in order to deal with complex protocols and timing of external interfaces. This philosophy should extend all the way out to board and system level interfaces. With the high levels of quality being demanded by customers, test capabilities could be a significant differentiator when function and performance are comparable. Because a significant amount of access is lost once the IP is integrated on to the chip, built-in test with consistent access is almost a requirement in order to achieve high test quality. While the cost to implement these test features may seem high for the IP integrator, the cost of lower quality and more expensive test resources will far outweigh the initial investment.

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