Package Design for High Performance ICs

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The world of packaging has changed in last few years. One of the reasons for this change is the increase in the complexity of today's ICs. The I/O count has increased, the pad pitch has decreased and the number of high performance drivers in the chip has increased. Today, packaging an IC cannot be considered as an afterthought in the product development cycle because it plays an important role in the optimum functioning of the chip. It is no longer a routine task that was needed to finish the product development but an enabler for the product creation.

Philips had to deal with these changes also by adopting complex EDA tools for package design, by introducing changes to its design flow & methodology, by doing a lot of predevelopment & characterization of new packages etc. Today, product development for any high performance chip is a co-design process between a chip and a package designer. Several wire bond packages have been developed using new design process. In this presentation, the old & new design process will be discussed with a 596BGA wire bond package as an example. Flip chip design process will also be reviewed using a 1312BGA package as a vehicle. A comparison between the design processes of these two package technologies will be made. Characterization process for thermal and electrical performance of the package will be reviewed and how these issues impact the package design process will be analyzed. Also, trade offs and decisions made at each step will be highlighted. The talk will conclude by highlighting current limitations of the design and analysis tools.

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