Systems on Chips Design: System Manufacturer Point of View

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Abstract

This paper discusses the design, packaging and testing of complex systems used for cellular mobile applications.

1. Introduction

The increasing diversity of cellular mobile equipment as well as their enriching feature set places stringent requirements on the efficiency of the whole design process starting from requirements and ending to production ICs and systems, especially as the design time, size, cost and power consumption need to be minimized without sacrificing reliability. The trends towards miniaturization and integration of complex systems containing RF, analog and digital functions place tightening demands on design methods and tools, specification and IP block design outsourcing procedures, design reuse and portability, co-simulation and co-verification, packaging, design for test and testing etc.

2. Design and Tools

The design of large systems requires use of systematic top down design method to help to manage the complexity and find globally optimal solutions. The design environment needs to support seamless co-operation of all involved parties, from system to circuit and PWB designers, from software engineers to analog and digital designers, and from writers of system specifications to test engineers. The design tools need to support a wide variety and combinations of description languages and formats (C, System-C, VHDL, VHDL-AMS, Verilog, Spice etc.), examples being ADVanceMS and AMS-Designer mixed signal mixed level simulators.

In top down design process the design is stepwise refined (see Figure 1) so that it gradually becomes more detailed and less abstracted (e.g. algorithm > transfer function > coefficients > device values/ratios > physical dimension). The design should be mapped to the implementation technology only in the latest steps to support reuse, portability and shrinks.

The use of external IP design houses requires standardization of block interfaces (e.g. VSIA), specification and description formats (e.g. VHDL-AMS, EDIF, GDSII), harmonization of design flow and/or tools etc. As an example of an enhancement of the design process, the VHDL-AMS models developed by the system manufacturer in the top down design process can be used as executable block specifications for the IP designers. The IP designers can provide the actual IP blocks together with more accurate and calibrated VHDL-AMS models back to the system manufacturer, who can use these models in the bottom-up assembly and verification of the system (transistor level circuit simulation of systems is seldom feasible).

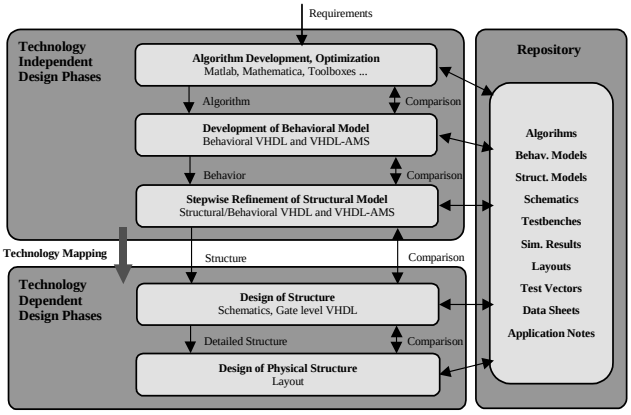

Figure 1. Stepwise refinement process in top down mixed signal design.

3. Packaging and Interconnections

Today portable systems use, for size and cost reasons, two to five levels of different interconnections/substrates such as system motherboard (typically PWB), module substrates or/and package interposers, one to two types of IC substrates (Si and GaAs) and sometimes also dedicated or surface mount compatible packages/interconnections inside specific modules (see Figure 2).

The use of increasing number of interconnecting substrates and various forms of packages/modules requires flexibility from the system design flow and tools. During the past 3 - 5 years the package and interconnection related system parasitics have changed remarkably: in the IC arena the tendency has been from lead frame to chip scale packages, and in passives from discretes to integrated arrays or chip form devices possibly with locally integrated ESD diodes.

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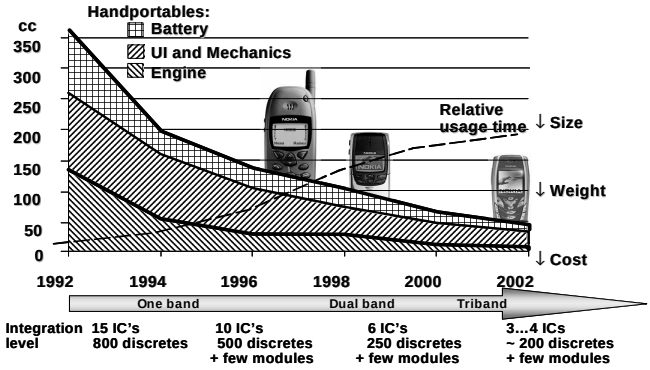

Figure 2. Progress in integration and modularity in cellular motherboard electronics vs. size, weight and cost of a cellular product.

Reducing the parasitics and loading (see Table 1) should help to minimize the power consumption in the interfaces. Still today chips to be stacked are very seldom electrically designed for stacking due to lacking interconnection models and their easy availability in the design flow.

Table 1. Parasitic capacitive and inductive elements of different interconnection methods.

	SMD package	BGA	Wire-bond	TAB	Solder bump
Capacitance (pF)	**1 ... 5**	**1 ... 2**	**0.5**	**0.6**	**0.1**
Inductance (nH)	**1 ... 12**	**2**	**0.5**	**1...2**	**0.01**

Increasing the number of cellular systems and bands in a product makes thermal design of multimode/–band RF challenging. If the power amplifier represents about 25 … 35 % of the dissipated power in a cellular product, the data centric multi-slot GSM is the worst case in terms of dissipated power for cellular RF (see Figure 3).

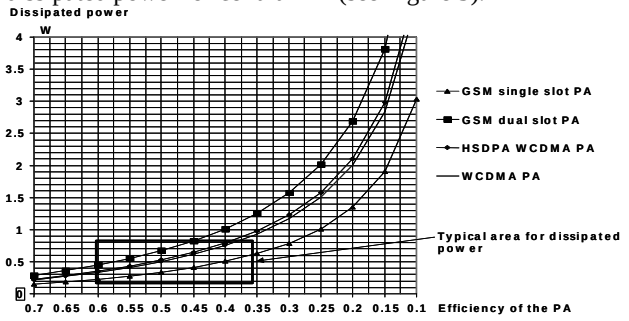

Figure 3. Dissipated power of cellular power amplifiers vs. their efficiency covering GSM, WCDMA and high-speed data packet access.

Increasing the number of applications, such as gaming and video streaming, increases the power dissipation of the digital parts. Packaging and motherboard interconnections need to provide thermal paths for the cellular electronics towards an acceptable and safe surface temperature of the product. In addition, the integration of analog and RF functions with digital logic brings along interference issues (common substrate, power supplies, package parasitics etc). With the increasing clock frequencies and number of devices in circuits, and the tighter specifications placed by the new systems and architectures, it becomes increasingly more important to be able to model and simulate the effects of the various interference mechanisms. Therefore, substrate and package modeling, in addition to substrate noise and thermal simulation software needs to be included in the design flow.

4. Test Design

Developing mixed signal IC test programs for ATE is a time-consuming task and should be done concurrently with the design cycle so as not to cause excessive delays in the IC verification. Today behavioral mixed signal modeling languages (VHDL-AMS etc.) and simulators enable the designer to generate a set of test vectors and stimuli, which can be used in the simulation phase as one simulation case and in the testing phase as one test case. Digital test vectors and analog waveforms can be automatically generated in correct tester format from the behavioral model simulation database (see Figure 4). Thus, the test environment can be developed at the same time with the IC's and the verification test can start immediately when the first prototypes arrive from the silicon foundry. Furthermore, the test quality can be improved as good testability can be built-in the systems during the design phase and the test vectors and stimuli can be more thoroughly verified. In the future, communicating test data wirelessly can further enhance testing.

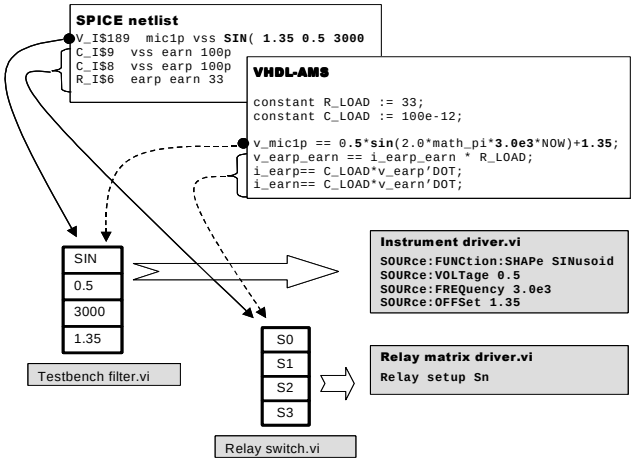

Figure 4. Generation of analog test stimuli.

5. Summary

To meet the challenges caused by tightening time schedules and cost pressures, as well as increasing diversity and complexity of systems the whole design process need to be continuously developed and improved. The design environment should seamlessly support IC and software design, packaging and PWB design, as well as test design and testing.