### A fast algorithm for the layout based electro-thermal simulation

M. Rencz, V. Székely, A.Poppe Budapest University of Technology and Economics, Hungary Rencz@eet.bme.hu

### Abstract

A new algorithm has been developed for the layout based direct electro-thermal simulation of integrated circuits. The advantage of the direct electro-thermal simulation over simulator coupling is, that very fast changes can also be considered, the drawback is that the thermal nodes are added to the number of nodes of the network to be simulated. The novelties of our method are the modeling and the solution of the thermal structure. This paper presents the algorithm of the time constant spectrum based FOSTER chain matrix thermal modeling, and the new algorithm of the coupled electro-thermal solution, where parts of the network, which represent the thermal behavior, are not computed in all steps of the iteration. This speeded up algorithm works both in the time-, and in the frequency domain. A simulation example demonstrates a typical application: the prediction of how the layout arrangement and the packaging of an analogue integrated circuit influence the electrical parameters.

## 1. Introduction

Due to the increasing component density and increasing speed the power density of VLSI circuits is continuously increasing, resulting in elevated chip temperatures and temperature gradients on the chip surfaces. Consequently, the operating temperature of the transistors at the different chip locations is different, resulting in different device parameters. Considerable temperature differences can be expected also as the result of the self-heating. Self-heating is crucial in the operation of SOI devices, or power devices of bulk technologies. To predict the temperature of the transistors during the operation, and during the transients requires accurate electro-thermal simulation, that considers not only the actual layout arrangement of the circuit, but as far as it is possible, even the effects of the packaging and cooling conditions of the realization.

In recent years increasing attention has been paid to the thermal issues in electronics design on system, board, package and chip level, including thermal and electrothermal simulation of integrated circuits and MCM-s, or MEMS. This trend is indicated by a considerable number of publications, see e.g. [1]-[10].

Most of these publications address the transistor level simulation by using SPICE, ELDO, SABER, or similar circuit simulators and a thermal simulator, that is usually a FEM program (e.g. ANSYS) connected in an iteration loop. One simulator uses the updated results of the other simulator in the iterative process. The method is called the *relaxation method*, the most important representatives are [3],[4] and [8]. The advantage is the relative simplicity of the implementation, the drawback is, that very fast changes can not be considered [6], and in case of strongly coupled thermal problems the simulator coupling frequently can not find convergence. Frequency domain calculation is usually not possible.

The other possibility for electro-thermal simulation is the *direct method* or simultaneous iteration. In these programs the thermal system is represented by an electrical model network, that has common nodes with the electrical-only network, the so-called *thermal nodes*. The iterative solution takes place simultaneously for the thermal and electrical sub-networks. Representatives of this method are discussed in [7], [9] and [12]. The advantage is the capability of considering very fast changes as well, the drawback is, that it requests a more complex implementation than the relaxation method [12].

Our department has a long-term experience in the investigation of the thermal behavior of integrated circuits. The first realization of direct electro-thermal circuit simulation was developed and published by our team [12]. This work resulted also in the development of a software package, called SISSI (Simulator for Integrated Structures by Simultaneous Iteration), that is aimed basically at electro-thermal simulation of analogue VLSI cells [13], [14]. The original version of this package was bound to a particular design kit of an industry standard IC design framework. This implementation allowed us to investigate a few benchmark problems: most of our circuits have been studied both by simulation, and after fabrication, by measurement [13]. In these case studies good agreement has been found between the simulated and measured results. The new thermal modeling and solution method presented here is aimed at the optimization of the solution time. In order to provide high level of flexibility and versatility, a design framework and technology independent realization is under development, but these issues are not discussed in the present paper.

The rest of the paper is organized as follows. In *Section 2* the principles of electro-thermal simulation are presented. *Section 3* gives the main contribution of the paper; the Foster chain matrix thermal model and the solution algorithm are presented here. In *Section 4* the capabilities of the method are demonstrated on a benchmark problem: the simulation of an operational amplifier. The results are evaluated in *Section 5*.

# 2. Principles and modeling questions of the direct electro-thermal simulation

### 2.1. **Principles**

As it was presented in the introduction, direct electrothermal simulation of the integrated circuits means, that electrical equivalent circuit models also the thermal behavior - determined by the geometrical sizes and the material parameters of the different components of the chip and the package. The electrical-only and the thermal equivalent circuits are connected in one network via the *thermal nodes*, the voltage of which represent temperature values. The two sub-networks form a large network for which the network equations have to be solved, providing simultaneously the temperature and voltage values of the thermal and electrical sub-networks respectively. The method raises the following new problems to be solved:

- (i) The device models have to be *electro-thermal*, they need to have a *thermal node* besides the electrical nodes. The instantaneous dissipation has to be forced to the thermal node as a current while the device function depends on the temperature (voltage) data of this node. This means, that the device model routines have to be rewritten keeping though as much as possible from the standard, e.g. SPICE-like device models, especially the parameters.
- (ii) The thermal behavior of the structure has to be modeled such, that is appropriate to be linked to the electrical solution algorithm and compact enough to provide a reasonably fast solution. The thermal model appears in the form of an electrical circuit, where electrical resistances and capacitances model the thermal resistances and capacitances, current models the heat flow and the voltage values represent the temperatures. A procedure has to be defined for the generation and insertion of the thermal models.
- (iii) An extended solution algorithm and/or strategy has to be used for the joint solution of the electrical and thermal parts of the investigated structure.

For the discussion below we have taken the following assumptions:

- (i) The thermal subsystem is considered to be linear.
- (ii) The algorithm of the electrical simulator is based on the nodal method. The solution of the non-linear system of equations follows a NEWTON-RAPHSON style algorithm.
- (iii) The time-domain integration (the transient solution) uses the reverse-EULER method.
- (iv) A lumped model substitutes the distributed thermal structure.

### 2.2. Compact Thermal Modeling

A possible and straightforward way of the modeling is to build a lumped RC model for the thermal structure using the finite difference method and to solve the electrical circuit and the electrical model of the thermal structure together. The appropriate modeling of the thermal part requires, however, a rather fine discretization. This means a huge number of nodes in the model network. Several thousands of nodes may be needed for the correct modeling of an IC chip. This considerable increase in the node number would result in a prohibitively long execution time. The best way to cope with this problem is to build *compact models* of the thermal subsystem. Several methods are known for this. The Asymptotic Waveform Evaluation (AWE) method calculates the moments of the thermal response from the discretised RC model by a recursive algorithm [5],[15]. Based on these moments a simple RC model network can be generated for each thermal port or thermal coupling. The Network Identification by Deconvolution (NID) method [16] uses the time- or frequency domain responses, pre-calculated by conventional thermal field-solvers [17] to generate the compact model of the system.

The concept of compact models is aimed at diminishing the number of nodes associated with the thermal subsystem but it is not capable to eliminate them completely. Our algorithmic contribution is that we separate the solution for the thermal nodes inside the thermal model and the solution for the remaining nodes, while the simultaneous iteration principle is kept intact.

# **3.** Thermal modeling with a matrix of Foster networks

Our novel idea for thermal modeling is presented in Fig.1. The dynamic thermal behavior of the *chip* + *package* thermal system is represented by an  $N \times N$  matrix of FOSTER RC chains, where N is the number of *coupling thermal nodes*. These nodes correspond to the footprints of the components considered to be thermally interactive on the chip. Each chain describes one element of the impedance matrix of the thermal structure. The chains will be indexed by the above-script indices n and m throughout the paper.

The FOSTER chains are defined by their time-constant sets and by the related magnitudes. These sets are generated by thermal simulation of the system. In our case this is done by the THERMAN program [17], but other 3D thermal field solvers are also applicable for this task.



Fig. 1 The two sub-networks and the coupling nodes

A characteristic property of this modeling approach is that although the model as a whole reflects correctly the behavior of the thermal structure, the individual R or C elements of the model can not be identified as mapping of a section of the physical structure.

### **3.1.** Modeling of a Single Thermal Impedance

The elements of the thermal impedance matrix may be either driving point or transfer impedances. The THERMAN program can be used also to calculate the discretised time constant spectrum for a thermal impedance. From the discretised time constant spectrum a



# Fig. 2 Foster chain is used to represent the thermal impedances

The R values are given by the amplitude values of the time constants, the C values are calculated from these and the time constants. Negative R values may also occur, since the network is fictive. In such cases the related C values are also negative. The length of the chains is variable. Typical lengths are between 1 and 5 but even zero length is possible in case of no coupling.

For solving the network problem we use the TRANS-TRAN program [12]. In the transient solution the TRANS-TRAN program uses reverse EULER integration. In this method the capacitors are substituted for each time step by parallel conductance-current source branches, where the current source represents the charge of the capacitor in the previous time step. For a Dt time step, the reverse EULER substitution of a given capacitor is presented in Fig. 3:



## Fig. 3 Substitution of the capacitors for the reverse Euler integration

where VC is the voltage of the capacitor in the current time value,  $VC_P$  was the voltage of the capacitor in the previous time instant. After this substitution the whole FOSTER chain looks as presented in Fig. 4, where the preceding voltages, that is, voltages in the previous time

instant of the transient analysis are denoted with  $VP_i$ .



#### Fig. 4 The Foster chain after substituting the capacitors

This network consists of a chain of resistors and a chain of generators. We store the resistance values of the  $n,m,\Delta t$  resistor chain in the  $RF_{i}$  vector as follows:

$$\stackrel{n,m,\Delta t}{RF}_{i} = \frac{1}{G_{i} + g_{i}} \tag{1}$$

where  $G_i = 1/R_i$  and  $g_i = C_i / \Delta t$ . The *i* index of the vector runs from 1 to *k* where *k* is the number of considered time

constants in the impedance, *n* and *m* are used as defined earlier: with the FOSTER chain indexed by *n* and *m* we describe the effect of the current of the *m*-th footprint on the *n*-th voltage.<sup>1</sup> The index  $\Delta t$  reminds us to the fact that for different time steps we have different *RF* vectors.

The currents calculated from these are  $\stackrel{n,m}{JP}_i$  (*i* = 1 ... *k* for both vectors).

$${}^{n,m}_{JP_{i}} = C_{i} \left( {}^{n,m}_{VP_{i}} - {}^{n,m}_{VP_{i+1}} \right) \frac{1}{\Delta t} \quad , \tag{2}$$

with  $\stackrel{n,m}{VP}_{k+1} = 0$ .

### **3.2.** Preparatory steps of the calculation

Let us investigate first a single chain. The terminal voltage and current of the chain are denoted by *VT* and *IT* respectively, see Fig. 5.



Fig. 5 The terminal current and voltage of the chain

To speed up the overall solution some data may be precalculated in advance and used later on, during the transient calculation, exploiting the fact that the chain is a linear circuit.

a.) Solution for the IT = 0 case while the JP generators are active. The V solution vector may be determined with the following recursive calculation:

$$V_{k}^{n,m} = RF_{k}^{n,m} \cdot JP_{k},$$

$$V_{p-1}^{n,m} = V_{p}^{n,m} + RF_{p-1} \cdot JP_{p-1}^{n,m}$$

$$n,m \land n,m \land n,m$$

Let this solution be denoted by  $VX_i$ .

b.) Calculation of the cumulative values of *RF* resistances:

$$RX_{k} = RF_{k}, \qquad (4)$$

$$RX_{p-1} = RX_{p} + RF_{p-1}.$$

According to the superposition theory we can state for the terminal node of the FOSTER chain that

$$VT = VT_0 + IT \cdot RT$$
(5)

where

$$VT_0 = VX_1$$
(6)

$$\begin{array}{l} n,m,\Delta t \\ RT = RX_1 \end{array}$$
 (7)

The above calculations have to be done for all the chains,

<sup>&</sup>lt;sup>1</sup> "Voltage" and "current" are applied for the temperature and the heat flow in the following discussion.

n = 1...N, m = 1...N. Finally the inverse matrix of RT will be calculated for further use:

$$GT^{n,m,\Delta t} = \begin{pmatrix} n,m,\Delta t \\ RT \end{pmatrix}^{-1}.$$
(8)

Eq. (3) has to be calculated when the iteration begins for a new time step. Eqs. (4), (7), and (8) have to be recalculated only if the time step of the solution is changed. Since during the time-domain integration usually a finite set of  $\Delta t$  step sizes is used, it is useful to store the pre-calculated data for all the  $\Delta t$  values and to fetch the appropriate ones if  $\Delta t$  has changed.

### **3.3.** Solution of the whole thermal model, the thermal N-port

Let us consider an N input thermal model, represented by the  $N \times N$  matrix of FOSTER chain model networks. Each of the FOSTER chains is described by Eq.(5), where n,m = $1 \dots N$ , giving one element of the impedance matrix of the thermal system each. Let the model input currents of the

whole model denoted by  $\overset{m}{J}$ , the voltages by  $\overset{n}{V}$ . In Eq.(5)

$$\stackrel{n,m}{IT} = \stackrel{m}{J}$$
 for any value of  $n$ , and  
 $\stackrel{n}{V} = \sum_{m=1}^{N} \stackrel{n,m}{VT}$ .

With these

$$\overset{n}{\boldsymbol{V}} = \sum_{m=1}^{N} \overset{n,m,\Delta t}{\boldsymbol{V}} T_{0} + \sum_{m=1}^{N} \overset{n,m,\Delta t}{\boldsymbol{R}} T \cdot \boldsymbol{J}$$

or

$$\mathbf{V} = \mathbf{V}_0 + \sum_{m=1}^{N} RT \cdot \mathbf{J}$$
(9)

where

Rearranging Eq.(9) results in

n,

$$\overset{p}{J} = \sum_{n=1}^{N} \overset{p,n,\Delta t}{GT} \cdot \begin{pmatrix} n & n,\Delta t \\ V - V_0 \end{pmatrix}$$
(11)

During the iteration for one  $\Delta t$  time step the solution for the model (the whole *N*-port) terminals is as follows:

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$$\overset{n}{V}$$
 vecto

- or the J vector may be (i) For a give obtained by using Eq. (11).
- The JACOBIAN matrix needed for the NEWTON-(ii) RAPHSON iteration is given by the inverse matrix  $n,m,\Delta t$ GT .
- (iii) Having the solution for the actual time step the "previous" voltages have to be updated for all the FOSTER chains, by

$$VP_i = VX_i + J \cdot RX_i \quad . \tag{12}$$

### 4. Example

The problem, simulated in this example is the benchmark example of Solomon [18], demonstrating the effect of the thermal feedback on operational amplifiers. As it was presented in [18] the thermal feedback results in characteristic distortions of the open loop transfer plots of operational amplifiers: double-humped open loop transfer curves are measured instead of the expected linear ones. Even the inversion of the slope may occur in certain regions of the transfer curve.

In Fig. 6 the investigated µA741 operational amplifier is presented. Only the current limiting transistors are omitted, not playing role in the thermal behavior.

The effect of the layout arrangement was studied for the most important 6 transistors T1,T2,T3,T4,T14,T20, these were modeled with electro-thermal models. The two layout arrangements of Fig. 7 were studied in details.



Fig. 6 The investigated benchmark example, the simplified **mA741** operational amplifier



Fig. 7 The examined two layout arrangements

Beyond the layout arrangement the effect of the packaging was also studied. In the structure of Fig. 8 we have varied the materials and the die attaching methodology according to the data of Table 1. These data have been introduced into the 3D field solver THERMAN for the calculation of the time-constant sets, needed for the model generation. First we examined the DC open loop V<sub>OUT</sub>(V<sub>IN</sub>) transfer characteristics. In Fig. 9 the transfer curves of the a.) layout arrangement are presented with different R<sub>L</sub> load resistors. Decreasing R<sub>L</sub> increases the current load of the output transistors, and consequently, their dissipated power, and the strength of the thermal feedback. If  $V_{0UT} > 0$ , the T14 transistor is dissipating, otherwise T20. As a result of the symmetrical layout arrangement these two transistors have opposite influence on the input transistors, this explains the opposite curvatures of the transfer functions. For the sake of comparison the result function of a pure electrical simulation is also plotted in the figure. The latter meets the expectations for a nearly ideal amplifier.



Fig. 8 The considered packaging structure Table 1.

	Layout	Die attach	Pad
1	a.)	glue 0.05 mm/2.5 W/mK	Kovar
2	b.)	glue 0.05 mm/2.5 W/mK	Kovar
3	a.)	solder 0.03 mm/50 W/mK	Kovar
4	a.)	solder 0.03 mm/50 W/mK	Cu



Fig. 9 DC transfer curves of the simulated op.amp., for the a.) layout arrangement of Fig. 7

Rearranging the output transistors asymmetrically on the layout, according to the insert, we obtain the transfer curves of Fig. 10.



Fig. 10 DC transfer curves of the simulated opamp, for the b.) layout arrangement of Fig. 7

Now the curvatures of the two parts of the plot are in the same direction, showing that in this arrangement both output transistors influence the input transistors similarly.

In our next experiment we have investigated the effects of the packaging on the thermal feedback. Cases 1, 3, and 4 of Table 1 were examined, for the same layout arrangement. The results are presented in Fig. 11. It is worth to note that the die attach method influences much less the electrical behavior, than the material of the pad. This example demonstrates that the effects of the thermal boundary conditions on the electrical behavior can be easily studied with the presented method.



Fig. 11 The effects of packaging on the DC transfer plot

The dynamic behavior is studied both in the frequency and the time domains. Fig. 12 shows the Bode plots of the open loop gain for the 1<sup>st</sup> and 4<sup>th</sup> case of Table 1, ( $V_{OUT}$  d.c. was 0.6V in both cases.) Note the significant differences in the Bode plots of the two cases.



Fig. 12 Bode plots of the open loop gain for two different packaging methods

In the transient simulation example, see Fig. 13, the open loop transients were examined, considering again the  $f^{st}$ and  $4^{th}$  case of Table 1, with 0.1mV step function input signal. As a result of the thermal feedback the output voltage of the  $1^{st}$  arrangement shows significant swinging before reaching the steady state.



Fig. 13 Transient curves for the case of the 1<sup>st</sup> and 4<sup>th</sup> layout and package arrangement (Table 1)

### 5. Conclusions

We have presented a methodology and an algorithm for the correct device/package level electro-thermal simulation of ICs. It is based on a novel representation of the thermal side, in which the elements of the thermal impedance matrix are represented by FOSTER type RC chains. This means, that the thermal model of the chip is a matrix of FOSTER type linear circuits.

An algorithm is presented for the most economic solution, in which parts of the circuit to be solved are precalculated and stored for later use, fastening up the total solution time to a convenient value.

Since the electrical solver uses sparse matrix techniques, the total solution time is surprisingly short, it takes  $O((E+N)^{1.2..1,5})$  time, where *E* is the number of the electrical, *N* is the number of the coupling thermal nodes. If *K* is the total number of the thermal nodes inside the model of the thermal part, we have to add to this the followings:

- At each changed Dt time increment calculation, that is, not more than 1-4 times during the transient simulation  $O(N^3)$  plus O(K) time is needed for data preparation.
- In every new time step O(K) and in every iteration  $O(N^2)$  calculation is the time need.

The total transient solution time need of the presented amplifier problem was about 2 sec on a PC - this can be considered immediate.

Electro-thermal simulators are strongly needed to analyze thermally operated MEMS structures that are expected to grow to the 30% of the total number of applied MEMS in the near future. To facilitate the simulation of these structures special models are needed for the convenient fast simulation: non-linear  $R_{th}$  model, Peltier element model, thermopile model, etc. We are currently working on the development of such models.

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