Transaction based design: Another Buzzword or the Solution to a Design Problem?

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Abstract

Complex systems on chip (SoCs) present challenges in the design and verification process that cannot be adequately addressed by traditional methodologies based on register transfer descriptions. Some of the aspects are efficient design exploration based on component reuse, getting closure on the architecture, as well as early development, integration and verification of embedded software. In search for responses to these challenges, Transaction level modeling (TLM) has got quite some attention in the area of SoC design. This panel attempts to do a reality check on TLM from an engineering point of view.

Questions to discuss are: Is the Transaction Level (TL) really useful for the design and/or for the verification of SoCs? How can TL speed up the design process and lowering the risk of design failures? What are the implications on tools, languages, and Intellectual Property (IP) used in the design/verification process? The panelists will share their thoughts on transaction based design and verification, and will discuss benefits and issues based on their experiences of applying transaction level methodologies.

Donatella Sciuto
Politecnico di Milano, Italy

Transaction-level modeling is one of the advances in system-level modeling that help system designers in the abstraction of the specification, allowing not bias the specification with implementation issues and focusing on the functionalities. Low level details of the implementation can be considered separately.

However, this allows higher level modeling and verification, but the gap existing with the implementation is quite big. I think that the real success of TLM will come when there will be, together with the modeling advantage, the support of tools and design flows for the refinement of the model into the best implementation for that particular specification. I don't think that today TLM allows a real speed-up in design, while it allows a speed-up in modeling and verification of the functionalities of the system.

Daniel Gajski
UC Irvine, USA

It is clear that higher abstraction levels can bring large productivity gains. The concepts of a channel and transaction level modeling are important and necessary but not sufficient features in system-level modeling. We have to learn how to use them; otherwise they will become just another buzzword.

The system-level research in the last 10 years demonstrated that large gains are possible if a systematic (axiomatic) approach is taken to system-level modeling, which will then result in simulatable, synthesizable and verifiable designs. Furthermore, it can be demonstrated that language wars are not necessary, since no new system-level language is needed to achieve the above goal.

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Carsten Mielenz
Infineon Technologies AG, Germany

Transaction-based design is an important design technology for embedded system designers. Our successful Virtual Prototype systems for architecture exploration and early software simulation are based on this technology. By approaching transaction-based design we could ease our IP modeling & reuse process and enhance the simulation speed of Virtual Prototype systems.

Christopher K. Lennard
ARM Ltd, UK

Transaction-based design is the cornerstone of the interface-based design principle - fundamental, but still a buzzword. Despite the emergence of interface synthesis, designers will continue to tune their IP towards a specific communication interface – hand-crafted, cycle-based piplined-interfaces are king when SoC execution speed is on the line. However, transaction based verification and validation (V&V) is here today.

Transaction-based testbenches are highly re-usable and intuitively modular, and transaction monitoring is the first step towards adequate SoC property and coverage checking. Transaction-based V&V is the small but vital step being taken towards the general vision of transaction-based design, and along with this are coming true improvements in the speed of accurate SoC simulation: improvements that the design productivity-gap demands.

Frank Ghenassia
STMicroelectronics, France

Register Transfer Level is the current VLSI design entry point. A decade ago, it was a major productivity booster vs. gate descriptions. It is commonly agreed that another entry point must be identified to bridge the gap between the number of transistors available on a chip and the ability for designers to exploit them. This next level entry point might well be the Transaction Level Model (TL or TLM) but synthesis from such description will remain a research topic for quite a while.

In the meantime, these TLM models can already be much more than a buzzword and become crucial for early software/firmware development, SoC functional verification and architecture exploration.

Stuart Swan
Cadence Design Systems, Inc., USA

It has commonly been assumed that one way to overcome the design and verification challenges posed by today's complex SoCs is to perform these tasks at higher levels of abstraction. However, until recently there have been several issues that have hindered the adoption of these new design flows. These include:

a) The lack of an industry-standard modeling language that could support this new design and verification process.

b) The lack of common modeling styles and design methodologies to facilitate IP exchange.

c) The lack of public endorsements from leading companies showing that these new design flows provide real benefits.

Today we are seeing that these issues have finally been resolved with the introduction of SystemC 2.0 and its associated standards, and with the SystemC transaction-level modeling capability that provides both very high performance and very high accuracy.

Joachim Kunkel
Synopsys Inc., USA

Describing systems at the transaction level in order to reap the benefits of more efficient modeling and faster simulation when designing complex systems is not new. What has changed recently though is that with the introduction of SystemC 2.0 the design community now has a design language with 'built in' support for transaction-level design.

The broad support network which SystemC enjoys today will accelerate the development of a 'standard' transaction-level methodology, very much in the same way as Verilog and VHDL did for the RTL methodology.

Once describing and simulating systems at the transaction-level has become an established design practice, transaction-level synthesis will become the next logical step.