Power/Ground Mesh Area Optimization Using Multigrid-based Technique

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Abstract

In this paper, we present a novel multigrid-based technique for power/ground mesh area optimization subject to reliability constraints. The multigrid-based technique is applied to reduce a large-scale mesh to a much coarser one. The reduced mesh can be efficiently optimized. The solution for the original mesh is then computed using a back-mapping process. Experimental results are very encouraging. Large-scale power/ground meshes with millions of nodes can be solved in a few minutes. The proposed technique not only speeds up the optimization process significantly without compromising the quality of solutions, but also brings up a possibility of incorporating the power/ground mesh optimization into other physical design stages such as signal routing.

1. Introduction

In today's high performance chip design, power/ground network synthesis is one of the most critical and challenging problems, especially with the continuous shrinking of process feature size and decreasing of noise margin. Power/ground network usually occupies a large portion of a chip area. To ensure the circuit performance and functionality, high-quality p/g network must be designed to utilize the chip area efficiently and eliminate potential electromigration reliability failures and excessive voltage drops.

Mesh is the most widely-used topology in p/g network design. The area optimization problem for a mesh topology has been shown to be non-convex and computationally hard ([6]). In the past, some heuristic techniques have been developed targeting this problem. Chowdhury [2] proposed a two-stage optimization process during which the current and voltage variables were fixed alternatively, and the resulting nonlinear programming problem was solved using the conjugate-gradient method. In [3], the original nonlinear problem was transformed into a sequence of linear programming (SLP) problems. Recently, [5] proposed a method of Incomplete Cholesky Decomposition Conjugate Gradient. In [6], a stochastic formulation was proposed and the cost function, which is a linear combination of the area and power consumption of the p/g network, is shown to be convex and solved effectively.

The previous methods have the following limitations:

1) They are applicable only to small circuit problems and unable to handle large-scale circuits. P/g networks in today's VLSI designs may contain millions of nodes and wire segments. In [4], the equivalent circuit model is adopted to simplify a large-scale network; however, this method can be applied only to a simple case of resistors in series. It is not suitable for general mesh structure.

2) Power/ground network optimization is usually carried out between placement and signal routing. The objective is to reserve more chip area resources for signal routing and at the same time maintain the performance of the p/g network. However, in the existing literature, p/g network optimization and signal routing are considered separately. In other words, during the p/g network optimization process, signal routing resource demand and router's utilization of the reserved chip area are unknown to the router. This causes difficulty in using the reserved chip routing resources. This problem can be alleviated if the p/g network design step could utilize the information obtained from after-placement congestion estimation. If in a particular region the routing congestion is high, we may allocate more space for signal routing there at the expense of the p/ g network and yet fulfill the reliability constraints.

In this paper, we propose a novel multigrid-based technique for p/g mesh area optimization subject to reliability constraints. Instead of optimizing a large-scale mesh itself, we reduce the original mesh by applying a multigrid technique. The reduced mesh can be optimized very efficiently due to its much smaller scale. The solution for the original mesh is then computed using a back-mapping process. The advantages of our technique are:

1) Significant speedup of the optimization process without compromising the solution quality.

2) Ability to combine p/g mesh optimization with other design stages such as signal or clock routing.

The rest of the paper is organized as follows: The problem formulation is described in section 2. In section 3 we review briefly the general multigrid method and its application in p/g network analysis. Section 4 gives an overview of our technique. Sections 5, 6, and 7 discuss the main three steps of our technique. Section 8 gives the experimental results followed by concluding remarks in section 9.

2. Problem Formulation

The problem formulation for p/g mesh area optimization subject to reliability constraints is stated as follows:

Given a power/ground mesh G with n nodes and b wire segments, each wire segment connecting two nodes, and each node may be associated with one current source, decide the width of each wire segment such that the area of G is minimized subject to the following constraints:

1) **Voltage drop constraints**. To ensure the correct logic operation, the voltage at each power mesh node should be close to the supply voltage:

 $V_{i} \ge V_{min}$ if node j is in a power mesh

$$V_i \le V_{max}$$
 if node *j* is in a ground mesh (EQ1)

2) **Current density constraints**. Electro-migration in a p/g wire segment sets an upper bound on the current density of the p/g edges. For a fixed thickness σ of a layer, this constraint for wire segment i can be expressed as $|I_i| \leq w_i \sigma$, and can be re-written as nodal voltage constraints:

$$\left|V_{i1} - V_{i2}\right| \le \rho I_i \sigma \tag{EQ2}$$

where ρ is the sheet resistance and l_i is the length of the wire segment.

3) **Minimum width constraints**. The widths of the p/g wire segments are limited by the process technology to the minimum width allowed in the layer. We have:

$$w_i \ge W_{MIN} \tag{EQ3}$$

4) Kirchoff's current law (KCL)

$$\sum_{i \in B(j)} s_i I_i = 0$$
(EQ4)

where B(j) are the indices of wire segments connected to a node *j*. If current direction in segment *i* is towards node *j* then s_i is 1, otherwise s_i is -1.

The objective of our technique is to allocate the chip routing resource consumed by p/g network as accurately as possible at the early physical design cycle, when the detail layout information is not available yet. The design of p/g network must be finished after performing accurate fullchip simulation and verification in the later design cycle when the detail layout parameters have already been extracted. We make the following assumptions:

1) We consider only mesh topology. At the beginning of a systematic p/g network design process, it is reasonable to have a regular structure such as mesh which can possibly be modified later into some irregular structure.

2) The p/g mesh is modeled as a resistive-only network, and the current loads are modeled as constant current sources.

3) An initial feasible solution is given, which means that the initial p/g network fulfills the reliability constraints, but it is over-designed with wide wire segments.

4) In the initial mesh, all the wire segments on the same horizental or vertical line have the same width. The usefulness of this assumption will be mentioned in section 5.2.

3. Multigrid Method

General multigrid method is an important technique for solving some special large scale problems. Due to the space limitations, we don't review it here, please refer to [9] and [10].

3.1 Multigrid Method for P/G Network Analysis

A multigrid-like technique was first applied for p/g network analysis in [7], then refined in [8]. The motivations of applying multigrid methods in p/g network analysis are:

1) Well-designed power grids are characterized by voltage distributions which are spatially smooth [7].

2) The system of linear equations resulting from the analysis of power networks is structurally identical to that of a finite element discretization of a two-dimensional PDE.

The analysis technique for p/g network proposed in [7] and [8] follows the steps of general multigrid method. The basic idea is to coarsen the p/g grid until the problem is small enough to be solved exactly using a direct approach, and to map the solution back to the original fine grid. Correspondingly there are three steps in that technique:

1) Grid reduction:

The objective is to remove as many nodes as possible while maintaining the ability to estimate voltage at the removed nodes.

2) Solving reduced grid:

The reduced grid can be solved exactly using a direct solver.

3) Interpolation:

The solution of the reduced grid is mapped back to the fine grid. The voltage at the removed nodes is estimated by interpolation based on the resistances to theirs neighboring nodes.

4. Overview of the Proposed Technique

The experimental results in [8] show that the multigridlike analysis technique provides very accurate simulation results for DC as well as transient analysis of the p/g mesh with the significant speed-up over traditional analysis techniques. In [7], an important property of the multigridlike technique for the case of mesh structure was stated: during the multigrid reduction process, the area (thus the resistance) of the entire p/g mesh is constant. From the point of view of circuit theory, the current sources of a p/g mesh are considered as circuit stimuli and the nodal voltages are considered as circuit responses. The total current drawn is unchanged during the reduction process; therefore to produce similar responses, the reduced mesh must have a similar resistance (thus area) to the original mesh. This constant area property constitutes the basis of our work explained in this paper. To apply the multigrid technique to the problem of p/g mesh area optimization, let us consider a particular instance. A feasible solution for the considered p/g mesh is a mesh with the given topology and decided wire segments widths, such that all the constraints are fulfilled. The set of all such solutions constitutes a feasible solution space for the initial grid, which is denoted as FSP. If we apply the multigrid reduction technique to every solution in FSP, we obtain the set of all reduced solutions, denoted as RFSP and called the reduced solution space. Every feasible solution in FSP can be mapped to a solution in RFSP. Because during the reduction process, the electrical characteristics are maintained by the multigrid technique, all solutions in RFSP are also feasible. Due to the constant area property of the reduction process, the reduced solution in RFSP mapped from the smallest area solution in FSP must also be the smallest area solution in RFSP. In other words, if we can find the optimal solution in RFSP, then by using a back-mapping process, we can determine the optimal solution in the original solution space FSP. Because the mesh after reduction is much coarser than the original mesh, the process of searching for the optimal solution in the reduced space is much easier than searching in the original space.

Our optimization technique follows the basic procedures of the general multigrid method. So we also have three steps, which will be discussed in detail in the following three sections:

- 1) Power/ground mesh reduction.
- 2) Solving the reduced mesh.
- 3) Back-mapping

5. Power/Ground Mesh Reduction

As suggested in [8], a natural method for efficient single level mesh reduction, inspired by the standard multigrid method, is to skip every other row/column. This yields significant reduction of the mesh topology because it reduces each of its dimensions roughly by half, thus reducing the whole mesh by almost a factor of four.

We follow and extend this simple approach in our mesh reduction algorithm to handle the general mesh structure, in which the distances between columns/rows and the widths of columns/rows may differ.

5.1 Reduction Matrix

As mentioned in section 2, an important property of the multigrid reduction process is that the entire area of the mesh is constant. In [10] a special case of a regular mesh was discussed. After skipping every other row/column, the width of each remaining row/column was doubled. This simple "doubling" approach is extended in our work to handle general mesh structure. During each level reduction, given the structure of the original mesh, we can immediately decide the structure of the reduced mesh by skipping every other row/column, and generating the relations between the width of the wire segments in the original mesh. These relations are expressed using two reduction matrixes, one for the row reduction and the other for the column reduction. The processes of constructing

these two matrices are the same, so we will discuss only the construction of the column reduction matrix.

Let us first consider the simple case of one level reduction. Suppose the number of columns in the original mesh is m, and the reduced mesh has m/2 columns. A is the column reduction $m/2 \times m$ matrix. The widths of the reduced mesh columns can be expressed as a linear combination of their original widths and the widths of their neighboring columns, now deleted, in the original mesh. Therefore, there is a total of m/2 linear equations. The reduction matrix A is the coefficient matrix of this set of linear equations. Each element in A is determined by the locations of the columns in the original mesh. Fig. 1 shows a simple case of removing only one column:



Fig. 1: A simple case

In the original mesh, the widths of columns a, b, and c are w_a , w_b , and w_c respectively. L_1 and L_2 are the distances from a to b and from b to c, respectively. After removing column b, in the reduced mesh, the widths of column a and b become w_a^* and w_c^* . To keep the total area unchanged, the increments of the widths can be expressed as follows:

$$\Delta w_{a} = w_{a}^{*} - w_{a} = w_{b} \cdot \frac{L_{2}}{L_{1} + L_{2}}$$
$$\Delta w_{c} = w_{c}^{*} - w_{c} = w_{b} \cdot \frac{L_{1}}{L_{1} + L_{2}}$$

The example in Fig.2 shows the complete construction process of column reduction matrix. We have the following set of linear equations:

$$\begin{vmatrix} 1 & \frac{I_2}{I_1 + I_2} & 0 & 0 & 0 \\ 0 & \frac{I_1}{I_1 + I_2} & 1 & \frac{I_4}{I_3 + I_4} & 0 \\ 0 & 0 & 0 & \frac{I_3}{I_3 + I_4} & 1 \end{vmatrix} \cdot \begin{bmatrix} \mathbf{w}_1 \\ \mathbf{w}_2 \\ \mathbf{w}_3 \\ \mathbf{w}_4 \\ \mathbf{w}_5 \end{bmatrix} = \begin{bmatrix} \mathbf{w}_1^* \\ \mathbf{w}_2^* \\ \mathbf{w}_3^* \end{bmatrix}$$

Please note that the above discussion is only applicable to single-level reduction. For the case of multi-level reduction, suppose *m* is the number of reduction levels, the original mesh is denoted as L_0 mesh, and after the *i*th $(1 \le i \le m)$ level reduction, the resulting mesh is denoted as L_i mesh. The reduction matrix associated with the L_i

mesh, ARM(*i*), is calculated as the product of all the previous single level reduction matrices:

$$ARM(i) = \prod_{j=0}^{i-1} A_{j \to j+1} \qquad (1 \le i \le m)$$
(EQ5)

where $A_{j \to j+1}$ is the one level reduction matrix from L_j mesh to L_{j+1} mesh. Specifically, when i = m, the final reduction matrix A_F is given by:

$$A_F = ARM(\mathbf{m}) = \prod_{j=0}^{m-1} A_{j \to j+1}$$
(EQ6)

We must point out that the constant area property holds explicitly only for the mesh structure. For a general topology, even though the constant area might be true in some cases, it is not a necessary condition. Besides, the multigrid reduction operation on a system matrix cannot be interpolated geometrically for an irregular grid [8].



5.2 Voltage Sources and Current Sources

An important problem is how to handle the voltage and current sources during the reduction process. As in [8], we keep the wire segments that have voltage sources attached so that the voltage sources always remain in the mesh during the reduction. Even in the flip-chip technology, the number of voltage sources in typical p/g mesh is much smaller compared to the total number of nodes. Therefore this restriction does not severely affect the efficiency of the reduction. A current source placed at a removed node, *i*, is split into current sources placed at the neighboring nodes from which *i* will be interpolated. The splitting will be proportional to the resistances (thus the distances if we take into account the last assumption made in section 2) between the node *i* and its neighboring nodes.

6. Optimizing Reduced Mesh

After the first step, the original mesh has been reduced to a coarser mesh. Any existing optimization method can be

used to search for the optimal solution for the reduced mesh. In this work, we adopt the sequence of linear programming (SLP) [5] method as the optimization engine.

The linear relations between W, the widths of the wire segments in the original mesh, and W^* , the widths of the wire segments in the reduced mesh can be expressed as:

$$A_F \cdot \mathscr{W} = \mathscr{W}^* \tag{EQ7}$$

 W^* is decided in this step by the optimization engine, and W is to be computed in the following back-mapping step. We notice that according to the minimum width constraints in the problem formulation, the above linear equations must have a solution whose each element is larger than W_{MIN} . However, if the optimization engine is unaware of this requirement, it may produce a solution of W^* for which there does not exist a W fulfilling the minimum width constraints. Therefore another set of constraints on W^* is needed such that the feasible solution of W is guaranteed.

Every equation in (EQ7) is of the following form:

$$\sum_{i=1} a_{ij} \cdot \mathbf{w}_i = \mathbf{w}^*_j \qquad j = 1 \dots \mathbf{u}$$
 (EQ8)

where *n* is the number of columns/rows in the original mesh and *m* is the number of columns/rows in the reduced mesh. a_{ij} is an element in A_F . We perform the following substitutions to (EQ8):

$$\sum_{i=1}^{n} a_{ij} \cdot x_i = b_j \qquad j = 1 \dots m$$

$$x_i = w_i - W_{MIN}$$

$$b_j = w^*_j - \left(\sum_{i=1}^n a_{ij}\right) W_{MIN}$$

$$X = \begin{bmatrix} x_1 \dots x_n \end{bmatrix}^T$$

$$B = \begin{bmatrix} b_1 \dots b_m \end{bmatrix}^T$$
(EQ9)

So the general formulation of our problem is:

given a set of linear equations:
$$A \cdot X - B$$

where A is an $m \times n$ matrix, X is an n-dimensional vector, and B is an m-dimensional vector. Every element in A is larger than or equal to zero.

We may ask, what is the sufficient condition for B such that X has at least one solution in which every x_i is larger than or equal to zero? For a general structure of A, finding the sufficient condition for vector B is not trivial. Fortunately in our problem, the reduction matrix A_F has two properties:

1) A_F is very sparse.

2) The number of variables present in the neighboring equations is very small.

Based on these two properties, it can be proved that the necessary and sufficient condition for B such that X has at least one solution in which every x_i is larger than or equal to zero is:

$$b_j \ge 0 \qquad j = 1 \dots m$$
 (EQ10)

thu

 $a_{j} \geq \left(\sum_{i=1}^{n} a_{ij}\right) W_{MIN}$ j = 1...m

Therefore, besides the constraints listed in section 2, the additional set of linear constraints (EQ11) must be taken into account during the SLP optimization process to find the optimal solution for the reduced mesh.

Please note that for any intermediate L_i mesh, there is also a set of additional linear constraints on its wire segments width, which can be similarly derived from the associated reduction matrix ARM(i) as we did for the final reduced mesh.

7. Back-mapping Process

Once the optimal solution for the reduced mesh is obtained from the optimization engine, the total area of the mesh is decided. The final step is to distribute the area into the original mesh by computing the solution for the original mesh using a back-mapping process. We limit the following discussion to computing the widths of all vertical wires.

It is imperative that the resulting solution for the original mesh is also feasible, which means all the reliability constraints have to be fulfilled. To achieve this objective and decrease the approximation error brought in by the reduction process, we adopt a corresponding multi-level backmapping process. During each level, a set of linear equations is solved. From L_i mesh to L_{i-1} mesh, the set of linear equations can be expressed using the one-level reduction matrix:

$$A_{i-1 \rightarrow i} \cdot W_{i-1} = W_i$$

where W_{i-1} and W_i are the vectors of column widths in the L_{i-1} mesh and L_i mesh respectively, and $A_{i-1 \rightarrow i}$ is the one level reduction matrix from L_{i-1} mesh to L_i mesh.

It is easy to notice that the above equations have more than one solution. This is so because multiple solutions for the L_{i-1} mesh can be reduced to the same solution for the L_i mesh. This property gives us a flexibility in choosing the configuration of the L_i mesh. Therefore the choice of the solution for the original mesh can be affected by some other design issues. As mentioned in the introduction, one approach is to combine p/g mesh area optimization with signal routing. Because by this time, module placement has usually been finished, we can utilize the resulting placement information to do congestion estimation using some existing techniques. For those chip regions with higher congestion, the p/g mesh should occupy a smaller area so that the routing overhead can be effectively reduced. On the other hand, for the regions with lower congestion, the p/g mesh can have a relatively larger area. We call this congestion-aware p/g mesh back-mapping. In our work, the one level back mapping problem is formulated as follows:

Congestion-aware back-mapping from L_i mesh to L_{i-1} mesh (i = m, ..., 1)

Given the nodal voltages and wire widths in L; mesh

Minimize
$$\sum_{j}^{N} \beta_{j} \cdot w^{j}_{i-1}$$

subject to:

(EQ11)

1)
$$A_{i-1 \rightarrow i} \cdot W_{i-1} = W_i$$
;

2)Between two neighboring horizontal (vertical) wire segments in L_i mesh, all the newly added vertical (horizontal) wire segments for L_{i-1} mesh on the same vertical (horizontal) line have the same width.

3)voltage drop constraints for all nodes in L_{i-1} mesh;

4)current density constraints for all segments in L_{i-1} mesh;

5)
$$W_{i-1}^{j} \ge \alpha_{i-1}^{j} \cdot W_{MIN}$$
 $(j = 1...N)$

In the above formulation, β_i is the weight coefficient assigned for each wire segment. It reflects the congestion situation where the wire segment is placed; larger β implies higher congestion. With the progressing of the back-mapping process, the congestion resolution can be gradually increased.

From EQ(1) and EQ(2), we observe that all the reliability constraints can be expressed as linear functions of the nodal voltages. By enforcing the constraint 2) in the above formulation and using interpolation, we can express the nodal voltages in L_{i-1} mesh using only the linear combination of the nodal voltages in L_i mesh and the topological information (length of wire segments), both of which are known. Therefore all the constraints in 3) and 4) are linear. Although constraint 2) may limit the solution space, this effect is inconsequential based on our experiments. The constraints in 5) come from the consideration that L_{i-1} mesh must be back mapped further to obtain the original mesh. All the α values in 5) can be computed from ARM(*i*-1), the associated reduction matrix of the L_{i-1} mesh as we discussed in section 6. Now we can conclude that the above one-level back-mapping problem is a linear programming problem that can be solved very efficiently. After solving this problem, the widths of the wire segments in L_{i-1} mesh are decided. To improve the accuracy, we simulate L_{i-1} mesh to update its nodal voltage values. The information about L_{i-1} mesh can be further used to solve the next-level back-mapping problem.

In summary, the back mapping process starts from the optimized final reduced mesh, and by solving the one level back-mapping problem from level to level, the optimal solution for the original mesh can be computed without violating any reliability constraints.

			SLP method		MGD reduction technique		
Circuit	# of nodes	# of edges	area reduced(%)	CPU time(s)	area reduced(%)	CPU time(s)	Speedup
m10x10	100	180	42.19%	11.78	41.87%	3.46	3.4
m20x20	400	760	51.89%	45.64	51.56%	5.31	8.6
m40x40	1600	3120	66.76%	329.78	67.01%	16.70	19.7
m100x100	10000	19800	88.34%	1401.52	85.66%	33.91	41.3
m1000x1000	1000000	1998000	N/A	N/A	72.27%	185.03	>194.5

TABLE 1. Comparison of our multigrid reduction technique against the SLP method

8. Experimental Results

We have developed our p/g optimization tool based on the proposed technique. For comparison, the sequence of linear programs (SLP) method [5] has also been implemented. All experiments were carried out on a PC running Linux with Pentium III 850MHz processor and 256MB memory. The results are summarized in Table 1. Columns 1 to 3 list the circuit name, number of nodes and number of wire segments. Columns 4 and 5 show the area reduction of the initial area in percentage for SLP, and CPU time in seconds for the SLP method, respectively. The area reduction technique are reported in column 6, 7 and 8. For each circuit, we provide the same initial mesh for our technique and SLP.

We make several observations based on the results shown in Table 1:

1) Our multigrid technique produces mesh areas similar or sometimes slightly smaller than the SLP method. To verify our resulting mesh, we run Hspice simulations. The results show that all the reliability constraints are indeed fulfilled.

2) Our technique is several orders of magnitude faster than the SLP method. The speedup is even more dramatic for larger circuits.

3) Our technique can handle truly large circuits. A mesh with 1000x1000 nodes can be solved in about 3 minutes. The SLP method cannot produce any result for this tested mesh even after running 10 hours.

Although in this paper, we have compared our technique only against the SLP method, our optimization engine can be implemented using any other method. No matter what kind of method we may use, our multigrid reduction technique can always speed up the optimization process because we need only to solve a much smaller mesh rather than the original large mesh.

9. Conclusions

In this paper, we have presented a novel multigrid-based technique for the power/ground mesh area optimization problem. With multigrid reduction, the optimal area of the p/g mesh can be quickly computed merely by performing optimization on the reduced mesh. The back-mapping pro-

cess to obtain the solution for the original mesh makes it possible to combine the p/g mesh optimization with other design stages such as signal routing. Using our technique, designers can quickly estimate the chip area consumed by p/g network at the early design cycle. Experimental results show that our technique is several times faster than the previous methods (up to hundreds of times faster), and can provide slightly better solution quality at the same time.

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