Test Generation for Acyclic Sequential Circuits with Single Stuck-at Fault Combinational ATPG

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1. Introduction

A test generation method with *time-expansion model* can achieve high fault efficiency for acyclic sequential circuits[1, 2]. While the model is combinational circuit, a single stuck-at fault in an original circuit is represented by a multiple one in this model. This paper proposes a test generation method for acyclic sequential circuits with a circuit model, called *MS-model*, which can express multiple stuck-at faults in time-expansion model as single stuck-at faults. Our procedure can generate test sequences for acyclic sequential circuits with just combinational test pattern generation algorithm for single stuck-at faults.

2. Multiple-to-single transformation

A circuit transformation to express a multiple stuck-at fault as a single stuck-at fault with an additional circuit is shown. Suppose a circuit C and a multiple stuck-at fault f^m consisting of two (single stuck-at) faults on lines a and b in C as shown in Fig. 1(a). (Note that a multiple fault is denoted by a variable with superscript m in this paper.) Here, we consider the following two transformations.

(1) Circuit transformation: For line a (b), a two-input gate G_a (G_b) is inserted and one input line of the gate G_a (G_b) is fed from the ground of C as a fanout branch of a ground line k (Fig. 1(b)). The inserted gate is determined according to the corresponding fault. The gate G_a is an AND gate whose input fed from line k is inverted when fault f_a is stuck-at-0, and the gate G_b is an OR gate when f_a is a stuck-at-1.

(2)Fault transformation: The multiple fault f^m is represented by a single stuck-at-1 fault f_s on the fanout stem k.

This pair of transformations is called *MS (multiple-to-single) transformation*, and a circuit model obtained by transforming a circuit C with a multiple fault f^m is called *MS-model* (of C) based on f^m. Note that an MS-model has no faults. Furthermore, note that MS transformation does not modify the design of given sequential circuits, but just generate circuit models for test generation.

In Fig. 1, the logic function of line a (b) is equivalent to the output function of gate G_a (G_b) because one input line of G_a (G_b), except a (b), is always fixed to logical 0. Namely, the inserted gates and lines composes a logically redundant sub-circuit for a MS-model.

3. TEM for acyclic sequential circuit

In test generation for acyclic sequential circuits using *time-expansion model* (TEM), first, a given acyclic sequential circuit S is transformed into a TEM $C(S)$[1, 2]. Fig. 2 shows an acyclic sequential circuit S. Lines *PI* and *PO* are a primary input and a primary output, respectively. Squares 1, 2, 3 and 4 are combinational logic blocks and rectangles *a*, *b*, *c*, *d* and *e* are registers. Fig. 3 shows a time-expansion model (TEM) $C(S)$ for S. TEM $C(S)$ is a combinational circuit derived by connecting logic blocks according to their sequential distances. A sequential distance between two blocks is defined by the number of registers on a path between the two blocks. (e.g, the sequential distance between logic block 3 and 4 is one.) If a logic block has several different sequential distances from another logic block in S, the logic block is duplicated in $C(S)$ (e.g., Logic block 2 has two different sequential distances to logic block 4 in S, two and three, and hence it is double in $C(S)$).

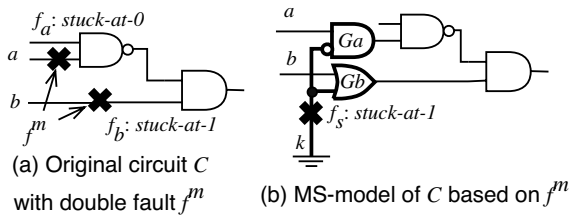

Figure 1. Example of MS-model

Since logic blocks are duplicated, it is needed to deal with multiple fault model even if the target faults are single faults. Suppose two single faults f_1 and f_2 in S (Fig. 2). The faults corresponding to f_1 and f_2 are f_{c1}^m and f_{c2}^m in $C(S)$, respectively (Fig. 3). As shown in Fig. 3, f_{c1}^m is a double fault consisting of all the faults existing on the same line in every logic block 1. Note that f_{c2}^m is still a single fault because the line on which fault f_2 exists is removed in one of logic blocks 2 duplicated in TEM $C(S)$.

4. MS transformation for TEM

As mentioned in Sect. 2, a multiple fault can be transformed into a single fault by MS transformation. Hence, a multiple fault in a TEM can be also transformed into a single fault with extra logics, and consequently a combinational ATPG that can deal only with single faults can be used for generating test sequences of single stuck-at faults in an acyclic sequential circuit. Fig. 4 illustrates the concept of such test generation approach. Suppose that an acyclic sequential circuit S with a single fault f is given. First, circuit S is transformed into a TEM $C(S)$. Single fault f in S is mapped into a multiple fault f_c^m in $C(S)$. Next, for multiple fault f_c^m, TEM $C(S)$ is transformed into an MS-model $C_{ms}(S, f)$ by MS circuit transformation. Furthermore, by MS fault transformation, multiple fault f_c^m is mapped into a single fault f_{ms} in $C_{ms}(S, f)$. We call an MS-model

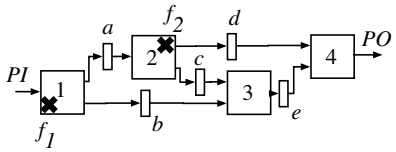

Figure 2. Acyclic sequential circuit: S

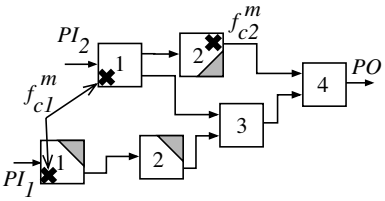

Figure 3. Time-expansion model: $C(S)$

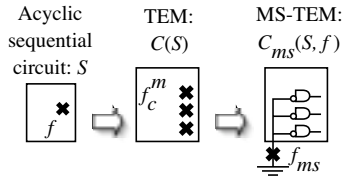

Figure 4. Circuit transformation and fault mapping

of a TEM *MS-TEM*. Note that $C_{ms}(S, f_c^m)$ is identical to $C_{ms}(S, f)$. Since MS-TEM $C_{ms}(S, f)$ is a combinational circuit, a test-pattern of single fault f_{ms} can be generated by a combinational ATPG that can deal only with single faults, and then the generated pattern can be transformed into a test sequence for fault f of S.

For a practical test generation approach using MS-TEM, we focus on the redundancy of the gates and lines inserted by MS circuit transformation. As mentioned in Sect. 2, the inserted gates and lines in an MS-model composes a redundant sub-circuit. Hence, it is possible to generate one MS-TEM that can express two multiple faults f_{c1}^m and f_{c2}^m in a TEM as two single faults f_{ms1} and f_{ms2} because the redundant inserted gates and lines for f_{ms1} does not affect test generation for f_{ms2}, and vice versa. Consequently, *any* number of faults in a circuit S can be expressed by one MS-TEM. Here, we extend the definition of MS-TEM $C_{ms}(S, f)$ that can only express a fault into $C_{ms}(S, F)$ that can express several faults $f_1, f_2, \ldots, f_n \in F$.

5. Equivalence fault collapsing

Equivalence fault collapsing according to the logic function of a logic gate is conventionally used in order to reduce the number of the target faults. This fault collapsing targets only faults on the inputs and the outputs of an logic gate. For example, for an AND gate, a stuck-at-0 fault on an input of the AND gate is equivalent to a stuck-at-0 fault on the output of the AND gate, and hence a representative fault of these equivalent faults is left in a fault list and other faults are neglected. Here, we call this fault collapsing *local fault collapsing* for short. The equivalent faults identified by local fault collapsing in S are still equivalent in its TEM $C(S)$, even if there exist removed points at several logic blocks in a TEM as shown in Sect. 2.

Theorem 1[3]: Consider an acyclic sequential circuit S and its TEM $C(S)$. If single faults f_1 and f_2 in S are identified as equivalent by local fault collapsing, then multiple faults f_{c1}^m and f_{c2}^m in $C(S)$ corresponding to f_1 and f_2, respectively, are also equivalent.

According to Theorem 1, the number of faults targeted by our test generation procedure can be reduced by local fault collapsing for S. Consequently, the reduction of the target faults can reduce additive logics for modeling a multiple fault as a single fault in MS-TEM.

6. Experimental results

Our test generation procedure for this experiment is as follows. First, an acyclic sequential circuit S was derived from a logic-level ISCAS89 benchmark circuit, and it was transformed into TEM $C(S)$. A single fault set F for S, which was reduced by local fault collapsing, was converted into multiple fault set $F_{C(S)}^m$ for $C(S)$. Next, an MS-TEM $C_{ms}(S, F_S)$ and its single fault set $F_{C_{ms}(S,F_S)}$ were obtained from $C(S)$ and $F_{C(S)}^m$, and a test set for MS-TEM $C_{ms}(S, F_S)$ was generated by using a single stuck-at fault combinational ATPG based on [5].

Table 1. Test generation results

	Proposed method		HITEC[4]	
circuit	eff[%]	time[sec.]	eff[%]	time[sec.]
s1196	100	1.17	100	0.05
s1238	100	1.77	100	0.76
s1423	100	0.25	99.8	9.56
s5378	97.19	1377.79	99.3	278.93
s9234	99.88	165.00	98.0	388.06

Table 1 shows the results of the proposed test generation method and sequential test generator HITEC[4]. This table shows the fault efficiency (eff) and the computational time in second (time). The fault efficiency is given by $(\#det + \#red)/\#fault \times 100$. The computational time of the proposed method includes the time for transforming an acyclic sequential circuit into a MS-model.

Comparing the proposed method with HITEC, the fault efficiency by the proposed method is equal or higher than that by HITEC for all circuits except s5378, while the computational time of the proposed method is comparable to that of HITEC. In particular, for s1423 and s9234, the proposed method can provide test sequences with higher fault efficiency in smaller computational effort than HITEC.

7. Conclusion

This paper presented a method for generating test sequences for acyclic sequential circuits using single stuck-at fault combinational ATPG. Experimental results show our method can generate test sequences in equal or lower computational effort than a conventional test generator for sequential circuits.

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