Improved Design Methodology for High-Speed High-Accuracy Current Steering D/A Converters

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Abstract

This paper describes a sizing and design methodology for high-speed high-accuracy current steering D/A converters taking into account mismatching in all the transistors of the current source cell. The presented method allows a more accurate selection of the optimal design point without introducing arbitrary safety margins, as was done in the previous literature. This methodology has been applied to the design of a CMOS 12-bit 400 MHz current-steering segmented D/A converter. Commercial CAD tools are used to automatically lay out regular structures of the DAC, specially the current source array, following an optimal two-dimensional switching scheme to compensate for systematic mismatch errors.

1 Introduction

High-accuracy (≥ 12 bits) and high-speed (from tens up to several hundreds of MHz) D/A converters (DAC) are required by modern telecommunication systems [1]. A CMOS current-steering DAC is the usual choice for this type of applications since this topology best suits those requirements. Fig. 1 shows a typical block diagram of a *n*-bits current-steering DAC. The input word is segmented between the *b* less significant bits, that switch a binary weighted array, and the $m = n - b$ most significant bits, that control the switching of a unary current source array. The *m* input bits are thermometer decoded to switch individually each of the 2^m-1 unary sources. A dummy decoder is placed in the binary weighted input path to equalize the delay. A latch is placed just before the switch transistors of each current source to minimize any timing error. The latches and switches are grouped in a separated array placed between the decoders and the current source arrays to isolate these noisy digital circuits from the sensitive analog circuits that generate the current.

The performance of the DAC is specified through static parameters: Integral Non Linearity (INL), Differential Non Linearity (DNL), and parametric yield; and dynamic parameters: glitch energy, settling time and SFDR [2]. Static performance is mainly dominated by systematic and random errors. Systematic errors caused by process, temperature and electrical slow variation gradients are almost cancelled by proper layout techniques [3]. Random errors are determined solely by mismatch due to fast variation gradients.

The design of current-steering DAC starts with an architectural selection to find the optimum segmentation ratio (*m* over *n*) that minimizes the overall digital and analog area [4,5,6]. The INL is independent of the segmentation ratio and depends only on mismatching if the output impedance is made large enough [7]. The DNL specification depends on the segmentation ratio but it is always satisfied provided that the INL is below 0.5 LSB for reasonable segmentation ratios. The glitch energy is determined by the number of binary bits *b*, being the optimum architecture in this sense a totally unary DAC. However this is unfeasible in practice due to the large area and delay that the thermometer decoder would exhibit. The minimization of the glitch energy is then bypassed to the circuit level design of the switch & latch array and current source cell.

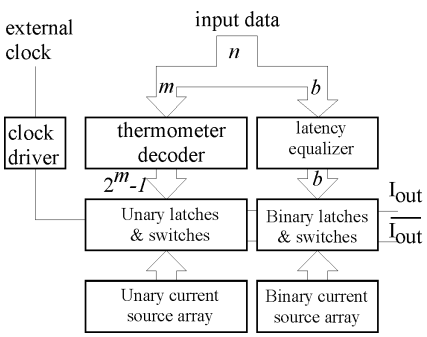

Fig. 1: Current-steering DAC architecture

After the architecture level optimization, the LSB current source cell must be optimally sized at circuit level taking into account the INL specification and trying to minimize settling time and to maximize output impedance. The other sources are scaled from it accordingly to its weight. In this paper an optimum sizing strategy for the current source cell is presented that complements previous approaches by taking into account matching errors not only in the current source transistor but in the rest of transistors of the cell as well. The optimization methodology is described in section 2. In section 3 this methodology is applied to the design a 12-bit current-steering DAC. Systematic mismatch errors are compensated at the layout phase, presented in Section 4 where the design techniques used to automatically lay out the regular structures of the DAC, specially the current source

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array following an optimal two-dimensional switching scheme to compensate for systematic mismatch errors, are addressed. Section 5 contains the conclusions.

2 Sizing strategy

There are two usual topologies for the basic current source cell, shown in Fig. 2. Topology (a) consists of a current source (CS) transistor and two complementary switch (SW) transistors. Topology (b) includes an additional cascode transistor (CAS) that increases the output impedance to fulfil the SFDR specification for resolutions ≥ 12 bits [8]. This later topology reduces the clock feedthrough from the switches to the drain of the CS thus reducing the glitch energy. A driver circuit with a reduced swing placed between the latch and the switch reduces the clock feedthrough to the output node as well. The latch circuit complementary output levels and crossing point are designed to minimize glitches.[9].

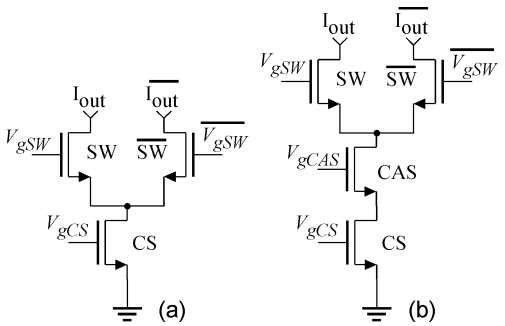

Fig. 2: Current source cell topologies

Table 1 shows the circuit level parameters (size and gate voltage) to be found by means of the optimization process for the topology (b) in Fig. 2. The aspect ratio W/L fixes the overdrive voltage (V_{gs}-V_T), and viceversa, for each transistor and for a given current I. The same aspect ratio can be obtained for different areas $W \times L$, except for the CS transistor, because the usual INL-mismatch specification eliminates one degree of freedom.

Current source (CS)	Switch (SW)	Cascode (CAS)
W_{CS}, L_{CS}, V_{gCS}	W_{SW}, L_{SW}, V_{gSW}	W_{CAS}, L_{CAS}, V_{gCAS}

Tab. 1: Current cell transistor level parameters

The relative standard deviation of a unit current source $\sigma(I)/I$ has to be small enough to fulfil the INL < 0.5 LSB specification given a parametric *yield* [10]:

$$\frac{\sigma(I)}{I} \le \frac{1}{2C\sqrt{2^{n-1}}}, \text{ with } C = \textbf{inv\_norm}\left(0.5 + \frac{yield}{2}\right), \quad (1)$$

where **inv_norm** is the inverse cumulative normal distribution. The CS transistor size is found by:

$$W_{CS}^2 = \frac{I}{K'\left(\frac{\sigma(I)}{I}\right)^2}\left[\frac{A_\beta^2}{(V_{gs}-V_T)_{CS}^2} + \frac{4A_{VT}^2}{(V_{gs}-V_T)_{CS}^4}\right]$$
$$L_{CS}^2 = \frac{K'}{4I\left(\frac{\sigma(I)}{I}\right)^2}\left[A_\beta^2(V_{gs}-V_T)_{CS}^2 + 4A_{VT}^2\right], \quad (2)$$

where K' is the MOS transistor gain factor, V_T the threshold voltage, and A_β and A_{VT} are their technology matching parameters, respectively.

2.1 Basic current cell (CS + SW) sizing

The overdrive voltage $(V_{gs}$-$V_T)_{CS}$ in (2) has to be maximized to minimize the CS area, but has to be small enough to allow the other transistors (SW and CAS, if present) to work in saturation in any situation to obtain the highest possible output impedance. For the current source in Fig. 2(a), the condition for the SW gate voltage that guarantees that both transistors operate in saturation is:

$$\underbrace{V_{OD}^{CS} + V_{OD}^{SW} + V_T^{SW}}_{V_{gSW}^{\min}} < V_{gSW} < \underbrace{V_o^{\min} + V_T^{SW}}_{V_{gSW}^{\max}}, \quad (3)$$

where V_{OD} are the overdrive voltages for the different transistors, and $V_o^{\min}$ is the minimum output voltage. A solution exists in eq. (3) if and only if the upper bound is greater than the lower bound. This determines an a saturation condition which bounds overdrive voltages addition in the worst case when $I_{out}R_L = V_o = V_o^{\min}$:

$$V_{OD}^{CS} + V_{OD}^{SW} \le V_o^{\min}, \quad (4)$$

from which the minimum area transistors will be obtained when the left part is equal to the right part. The last two expressions relate the SW and the CS transistors overdrive voltages in such a way that if one of them is fixed, the other one is derived using eq. (4). The CS transistor is the larger of the two, so its overdrive voltage is always fixed to the highest possible value fulfilling eq. (4). By doing this, the overdrive voltage of both transistors is found just at the limit between the triode and the saturation regions. In the sizing procedure previously reported [9,11] an arbitrary safety margin is introduced in eq. (4) to prevent the transistors to enter triode region due to process variations: $V_{OD}^{CS} + V_{OD}^{SW} = V_o^{\min} - \Delta V_{safe}$.

Additionally, the CS gate voltage is intrinsically determined by its overdrive voltage. It can be easily shown that the maximum of the DC output impedance when channel length modulation is taken into account is found when the SW gate voltage is:

$$V_{gSW}^{opt} = V_T^{SW} + \frac{1}{2}\left(V_o^{\min} + V_{OD}^{CS} + V_{OD}^{SW}\right) = \frac{V_{gSW}^{\max} + V_{gSW}^{\min}}{2}. \quad (5)$$

If the mismatch error of the switches and additional cascode transistors is taken into account the overall basic

current cell circuit can be optimised without introducing the arbitrary safety margin (ΔV_{safe}) as is shown in the following.

In the proposed sizing procedure the whole range of possible CS and SW overdrive voltages that verify (4) is explored including process variations. For each pair $\left(V_{OD}^{CS}, V_{OD}^{SW}\right)$ the minimum area and aspect ratio of the CS transistor is found using eq. (2). If the length of the SW transistor is chosen to be minimum (this is done to maximize the switching speed) the area and aspect ratio of the SW transistor are found from the SW overdrive voltage and the *I* current value. The settling time in this type of converters is approximated by the time constant of the lower frequency of one of two real poles, the first corresponding to the output node and the second corresponding to the internal node. The poles frequency can be represented against $\left(V_{OD}^{CS}, V_{OD}^{SW}\right)$ or other equivalent transistor parameters to choose the optimum sizing if settling time is the most important concern, as it is shown in the next section. Indeed, other parameters (output impedance, total area) may be used instead as the optimization goal depending on the system requirements.

In order to include in the previous analysis the effect of process variations in the SW, the statistical variation of the two bounds for the SW gate voltage in eq. (3) is modeled by means of a Gaussian distribution. The variance of the upper bound is found by expressing $V_o^{\min}$ as a function of the LSB current *I*, load resistance R_L, and V_T^{SW}, and taking partial derivatives:

$$\sigma^2_{V_{gSW}^{\max}} \approx \left(\frac{\partial V_{gSW}^{\max}}{\partial I}\right)^2 \sigma_I^2 + \left(\frac{\partial V_{gSW}^{\max}}{\partial V_T^{SW}}\right)^2 \sigma^2_{V_T^{SW}} + \left(\frac{\partial V_{gSW}^{\max}}{\partial R_L}\right)^2 \sigma^2_{R_L} = \\ = \frac{A_{VT}^2}{W_{SW}L_{SW}} + \left(V_{DD} - V_o^{\min}\right)^2 \left(\frac{\sigma_I^2}{I^2} + \frac{\sigma^2_{R_L}}{R_L^2}\right) \quad (6)$$

Similarly the variance of the lower bound yields:

$$\sigma^2_{V_{gSW}^{\min}} \approx \frac{A_{VT}^2}{W_{CS}L_{CS}} + \frac{A_{VT}^2}{W_{SW}L_{SW}} + \frac{V_{OD}^{SW\,2}}{4}\left(\frac{\sigma_I^2}{I^2} + \frac{A_\beta^2}{W_{SW}L_{SW}K'^2}\right). \quad (7)$$

To find an appropriate value for the SW gate voltage, the upper bound must be larger than the lower bound in a given percentage of the cases expressed by *yield_SW*. If this is accomplished, the optimum of the SW gate voltage found in (5) has to verify that:

$$p\left(\left[V_{gSW}^{\max} - V_{gSW}^{opt}\right] > 0\right) \geq yield\_SW \text{ and} \\ p\left(\left[V_{gSW}^{opt} - V_{gSW}^{\min}\right] > 0\right) \geq yield\_SW \quad . \quad (8)$$

This is translated into an new saturation condition:

$$V_{OD}^{CS} + V_{OD}^{SW} = V_o^{\min} - 2S\max\left[\sigma_{V_{gSW}^{\max}}, \sigma_{V_{gSW}^{\min}}\right]; \quad (9)$$

here, since only one half of the Gaussian distribution has to be considered, $S =$ **inv_norm**$(yield\_SW)$ where *yield_SW* is related to the INL *yield* by $yield = yield\_SW^4$, because the LSB current cell is the worst case (its area is the smallest of all the current sources) and its two complementary SW transistors must be both inside the two bounds with the same probability.

The expression of eq. (9) represents a saturation constraint more realistic than eq. (4) where an arbitrary safety margin has to be included. To minimize the overall area the $\left(V_{OD}^{CS}, V_{OD}^{SW}\right)$ pair is always chosen along the saturation condition lines in the upper graph of Fig. 3, that compares the saturation conditions of eq. (4) and (9). The 500 mV arbitrary safety margin always gives overdrive voltages smaller (it is, larger transistor areas) than the new saturation condition presented in this section.

2.2 Cascode current cell (CS+CAS+SW) sizing

If an additional cascode transistor is inserted as shown in Fig. 2(b) the previous analysis is applied to both the SW and the CAS transistors in the same way. The optimum of the DC output impedance is found in this case when the SW and CAS gate voltages are:

$$V_{gCAS}^{opt} = V_T^{CAS} + \frac{1}{3}\left[V_o^{\min} + 2V_{OD}^{CS} + 2V_{OD}^{CAS} - V_{OD}^{SW}\right] \\ V_{gSW}^{opt} = V_T^{SW} + \frac{1}{3}\left[2\left(V_o^{\min}\right) + V_{OD}^{CS} + V_{OD}^{CAS} + V_{OD}^{SW}\right] \quad . \quad (10)$$

The CAS transistor introduces two new degrees of freedom: its overdrive voltage and its area (or channel length). One of these two degrees of freedom can be eliminated as explained in [8] using an output impedance/bandwidth criterion by relating the sizes of the SW and the CAS transistors. Another possible criterion is to choose the minimum width for the CAS transistor which, in addition to minimise the CAS transistor area, also minimises the parasitic capacitance at the source of the SW transistors hence yielding a reduced settling time (assuming that the pole due to this node is the limiting one). Therefore, the area (or dimensions) of the CAS transistor is determined univocally by its overdrive voltage and the current *I*.

In this case the range of SW and CAS overdrive voltages that guarantee saturation is found by solving (9) for the two transistors. This yields to two saturation conditions, if statistical variations are taken into account, which is now a limit surface in the 3D-design space:

$$V_{OD}^{CS} + V_{OD}^{CAS} + V_{OD}^{SW} \leq V_o^{\min} - 3S\sigma_{bound}^{\max}; \quad (11)$$

with $\sigma_{bound}^{\max} = \max\left[\sigma_{V_{gSW}^{\max}}, \sigma_{V_{gSW}^{\min}}, \sigma_{V_{gCAS}^{\max}}, \sigma_{V_{gCAS}^{\min}}\right]$ as the maximum variance of the four bounds, where the SW and CAS gate voltage bounds statistical variances due to process variations have the expressions:

$$\sigma^2_{V_{gSW}^{\max}} \approx \frac{A_{VT}^2}{W_{SW}L_{SW}} + \left(V_{DD} - V_o^{\min}\right)^2 \left(\frac{\sigma_I^2}{I^2} + \frac{\sigma_{R_L}^2}{R_L^2}\right)$$

$$\sigma^2_{V_{gSW}^{\min}} \approx \frac{A_{VT}^2}{W_{SW}L_{SW}} + \frac{A_{VT}^2}{W_{CAS}L_{CAS}} + \frac{V_{OD}^{SW\,2}}{4}\left(\frac{\sigma_I^2}{I^2} + \frac{A_\beta^2}{W_{SW}L_{SW}K'^2}\right) \quad (12)$$

$$\sigma^2_{V_{gCAS}^{\max}} \approx \frac{A_{VT}^2}{W_{SW}L_{SW}} + \frac{A_{VT}^2}{W_{CAS}L_{CAS}} + \frac{V_{OD}^{SW\,2}}{4}\left(\frac{\sigma_I^2}{I^2} + \frac{A_\beta^2}{W_{SW}L_{SW}K'^2}\right)$$

$$\sigma^2_{V_{gCAS}^{\min}} \approx \frac{A_{VT}^2}{W_{CS}L_{CS}} + \frac{A_{VT}^2}{W_{CAS}L_{CAS}} + \frac{V_{OD}^{CAS\,2}}{4}\left(\frac{\sigma_I^2}{I^2} + \frac{A_\beta^2}{W_{CAS}L_{CAS}K'^2}\right)$$

3 Optimum sizing of a 12 bits current-steering DAC

The optimization process described in the above section has been implemented in Matlab and applied to the design of a 12 bits DAC. The target technology is a 0.35µm CMOS process. The segmentation has been set to b= 4 and m = 8 bits, V_{DD} = 3.3V, $\Delta V_o^{\max} = 1$ V and R_L = 50Ω. The internal node interconnection capacitance has been estimated to be 100 fF, and the output capacitance 2 pF.

If the basic current source topology is chosen (CS+SW transistors) any optimization parameter can be represented against the two degrees of freedom available (for example, the two transistors overdrive voltage, or alternatively their corresponding area). Fig. 3 shows graphs representing optimum sizing for two criteria (area and settling time). The upper graph compares the saturation constraints, whilst the lower graph shows the minimum of the pole frequency against CS and SW overdrive voltages and a couple of optimum design points. The first pole (p_1) is due to the output load and the parasitic capacitance at the drain of all the switch transistors connected to the output (that will increase with its width). The second pole (p_2), due to the internal node, has contributions of both the parasitic capacitance of the CS drain and the SW source, and depends on the SW transistor small signal trasconductance and body effect parameters, as presented in [9]:

$$p_1 \approx \frac{1}{2\pi R_L\left(C_L + C_{draintot}^{SW}\right)}$$

$$p_2 \approx \frac{g_m^{SW} + g_{mb}^{SW}}{2\pi\left(C_{draintot}^{CS} + C_{gs}^{SW} + C_{int}\right)} \quad (13)$$

In p_2 the interconnection capacitance between the switch & latch and the current source arrays C_{int} is taken into account [8]. The small signal parameters and parasitic capacitances determining the poles are known once the sizes of the transistors are found. The only degrees of freedom are the two transistors overdrive voltages and they univocally determine the transistor sizes, as discussed in section 2. Not all the combinations are possible, however, due to the constraint set by the saturation condition of eq. (9) that limits a region of the $\left(V_{OD}^{CS}, V_{OD}^{SW}\right)$ plane where the optimum design point should be found.

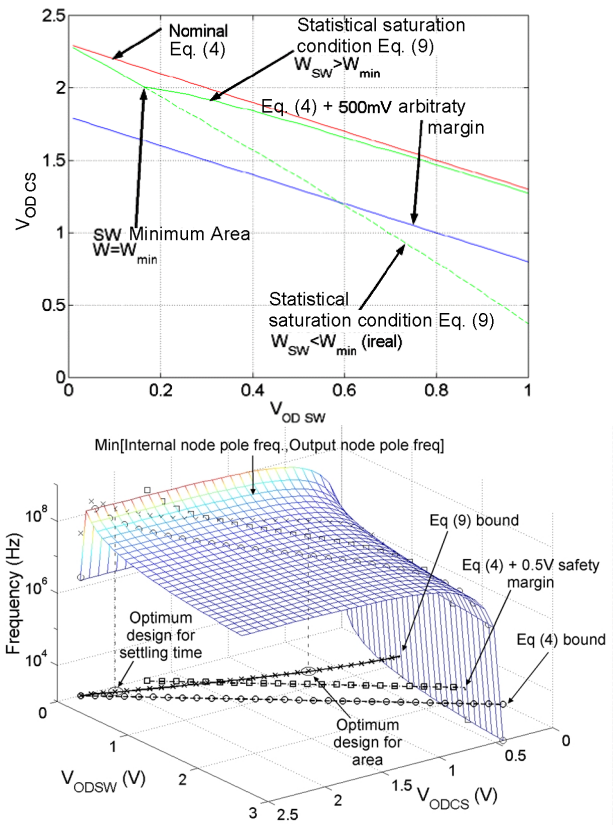

Fig.3: Optimization graphs for the SW+CS topology for a 12 bits DAC

For maximum speed the optimal design point is found where the minimum of the two poles frequency is maximized. If a minimum area is the preferred goal, the point in the $\left(V_{OD}^{CS}, V_{OD}^{SW}\right)$ plane inside the saturation condition constrained region with the lowest possible $Area^{CS} + Area^{SW}$ value should be chosen instead which will minimize the total area taking into account the matching constraint of eqs. (1) and (2). The saturation conditions used previously in the literature are also shown in Fig. 3 for comparison. The use of an arbitrary safety margin leads to inefficient solutions as shown in the figure.

The SW+CS topology does not provide enough output impedance for a 12-bit DAC and a cascode transistor has to be added. It is cumbersome to represent the optimization parameter (for example poles frequency) for the SW+CAS+CS topology, since a 4th dimension is required, so only the bounds for the overdrive voltages have been plotted in Fig. 4 for that topology. The design space that guarantees that all the transistors operate in saturation found by using eq. (11) is the volume under the surface. The bounds set by the

equivalent to eq. (4) for this circuit are also shown for comparison.

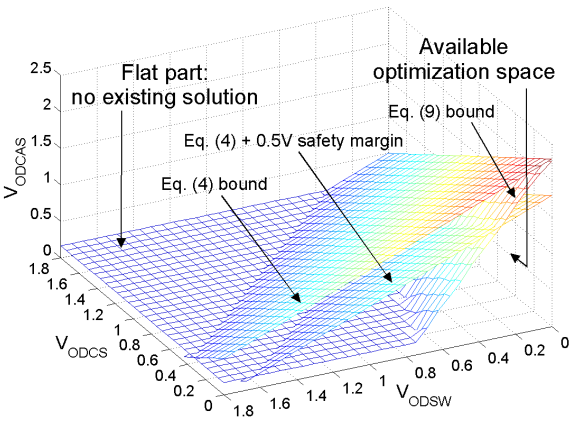

Fig. 4: Design space for the SW+CAS+CS topology for a 12-bit DAC

4 Physical design of the converter

The deterministic process-induced variations (systematic mismatch) produce systematic parameter fluctuations across the surface of the chip. The impact of this systematic parameter fluctuations is more severe in large regular structures of theoretically equal devices placed in array structures, as is the case of the current cells array of the current-steering D/A converters. In order to minimize the error in the output transfer function of the D/A converter some techniques can be used to compensate for the systematic parameter fluctuations. In this work the optimum switching-scheme presented at theoretical level in [3] has been used to lay out the current source array of the converter thermometer segment. Each current source transistor has been also divided in 16 sub units that have been placed following a double centroid distribution [12]. The overall architecture of the D/A converter is shown in Fig. 5. Each binary and unary bit has its own latch & switch block. They are placed in a separate array following also a local centroid distribution in groups of four. The binary latches & switches are placed in the middle of the array, and the binary current source transistors are also distributed in four dedicated columns of the current source array.

After the circuit sizing phase the basic blocks of the structures have been manually laid out from their schematic. A Cadence LEF format file [13] describing the relevant geometrical information for placement and routing is automatically generated from the layout for each block. Then, the switching sequence for the current source array, taking into account the special locations of the binary cells, is programmed in a C script that generates a file in the Cadence DEF format [13] that describes the placement of the cells and also their interconnection. The same interconnection scheme proposed in [12] based on three metal layers is used here. The DEF file also contains information about the placement and the routing of the latch & switch array. This approach allows easily adapting the design process to other requirements as the generation of the DEF file is completely parameterized.

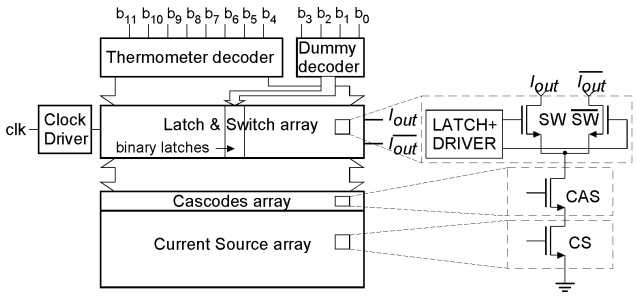

Fig. 5: Floorplan of the 12-bit DAC

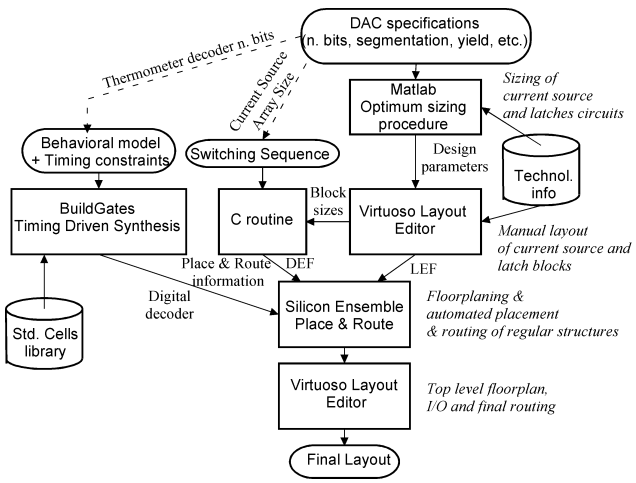

Fig. 6: Overview of the design process indicating the CAD tools used in each step.

The thermometer and dummy decoders have been automatically synthesized, placed and routed in a separate block using also Cadence tools and standard cells from the vendor library. This block is automatically routed to the latch & switch array. Finally the I/O circuitry and other top-level components have been semi automatically placed and routed using a layout editor (Fig. 6). The 12-bits DAC core layout is shown in Fig. 7. Simulation results at transistor level including all the parasitics extracted from the layout indicate an SFDR of approximately 40dB for a sinusoidal input of 53MHz sampled at 300MHz, which compares very well with state-of-the-art published 12-bit DACs [9]. The spectrum obtained by applying the DFT to 50 periods of the differential output waveform is shown in Fig. 8. IN this simulation, matching effects have been taking into account. The settling time for a full scale differential output swing is 2.5ns, as shown in the transient simulation result of fig. 6, allowing operation of this DAC up to 400 Msamples/s.

5 Conclusions

The presented sizing methodology and design sequence for high-speed high-accuracy current steering DACs, that complements previous approaches, avoids the introduction of an arbitrary safety margin for the overdrive voltages saturation condition by analyzing the effects of process variations in the operating region of all the transistors of the current cell. This allows further minimization of the total DAC area. The presented approach takes into account the mismatching effects to find a safe design space for the two most usual topologies of the current cell. The results shown in Fig. 3 indicate that, for the particular technology and DAC topology analyzed in this work, the proposed approach allows saving area in comparison with the approach of [9] where a 0.5V safety margin is added to the overdrive voltages bound. In this methodology square-law current equations have been used because the matching data provided by the manufacturer are intended for this transistor model. Indeed, the same methodology can be applied using more sophisticated transistor models to increase the accuracy provided that the process matching parameters are available also for these other models.

The proposed design methodology has been applied to the design and optimization of a high-performance 12-bit DAC. In the current source array an optimum switching sequence has been used to compensate for systematic mismatch errors. The complexity of the placement and routing of this structure has been solved using commercially available place & route tools. It is very important to preserve the regularity in the placement and routing structure above the current source array and between the switches and the current source transistors. This minimizes the possible mismatching due to the surrounding structures in the current source array and equalizes the interconnection length and capacitance for any current source transistor, minimizing in such a way the synchronization errors.

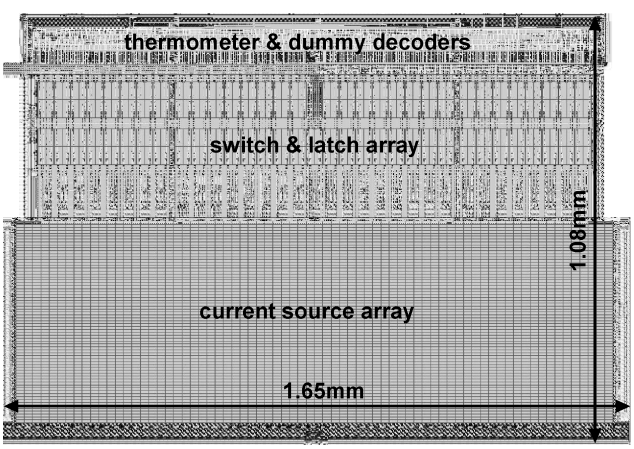

Fig. 7: Layout of the designed 12-bit DAC

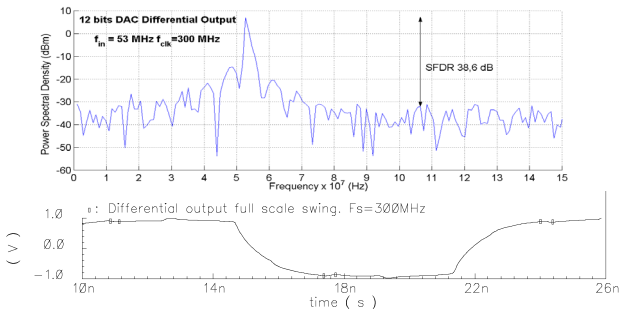

Fig. 8 Results of the designed 12-bit DAC

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