Linear model-based error identification and calibration for data converters

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Abstract

For the example of a 12-bit Nyquist-rate ADC, a model for nonlinearity-causing mechanisms is developed based on circuit simulations. The model is used to estimate circuit element values from measured device characteristics. Post-manufacture reconfiguration of the digital control part of the device-type that is used as a test vehicle in this work can improve the linearity performance of a device. An algorithm is proposed that searches for a locally-optimal reconfiguration based on the determined circuit element values. Applying calibration to the circuit simulation model allows one to estimate the performance improvement obtainable with the proposed calibration scheme for a given manufacturing process prior to a physical implementation.

1. Introduction

Traditional analog calibration strategies applied to data converters have been based on a "measure-trim-repeat" approach until the device either meets the specifications or the maximum number of allowable iterations is exceeded. This iterative approach resulted from the fact that individual device component values and the quantitative effect of the trimming action were unknown, due to access restrictions to the device.

In this work, we extend a model-based approach to ADC linearity test time reduction that was originally developed at the National Institute of Standards and Technology [3, 4] and has been demonstrated for the ADC used in this work [6]. Unlike in the test time reduction approach, we use a model that is invertible allowing one to estimate component values from the measured INL characteristic of an ADC device. Using the known component values, an algorithmic approach is presented to find calibration settings that improve device linearity.

Moreover, extracting the component values for a set of uncalibrated devices allows one to simulate the performance improvement obtainable using a given calibration scheme prior to committing to physically implementing this scheme.

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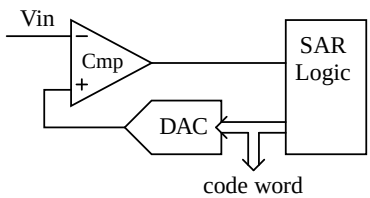

Figure 1. Successive Approximation Register feedback loop.

This is demonstrated for the example ADC indicating the improvements of the linearity performance that are obtainable with the calibration scheme used as an example here.

2. A priori modeling

The ADC we are using operates a 12-bit charge-redistribution DAC in a Successive Approximation Register (SAR) feedback loop for which a top-level schematic is shown in Fig. 1. The output code of the ADC is the DAC input "code word" for which the DAC output voltage matches the ADC input voltage.

Nonlinearities of the transfer characteristic are determined by error mechanisms in the ADC. These are nonlinearities of the DAC and non-idealities (such as insufficient settling of the comparator decision) of the feedback loop. We focus on reducing the DAC nonlinearities as they turn out to be the primary contributors to the nonlinearity of the ADC we are investigating.

Known error mechanisms in the DAC which impact the ADC nonlinearity characteristic, such as circuit element mismatches, can be simulated. From these simulations we derive a map of these error mechanisms to the ADC nonlinearity characteristic. Inverting this map, we identify the presence and magnitude of error mechanisms in manufactured devices for which measurements of the nonlinearity characteristic are available.

Based on the identified error mechanisms, values for the circuit elements are determined, parameterizing the simulation model of the ADC to fit the measured device characteristic. Hypothetical changes to the digital and/or analog part of the devices can be evaluated by applying these changes to the simulation model. In our case, this suggests that significant parasitic capacitance is present in the manufactured devices whose impact can be reduced by re-sizing one of the capacitors in the circuit design.

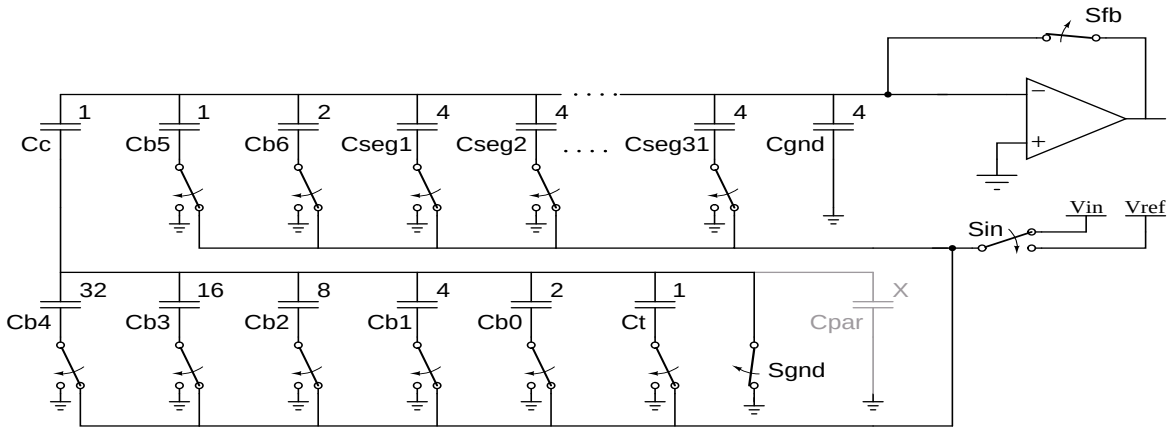

Figure 2. 12-bit charge-redistribution ADC core with top five bits segmented.

2.1. Simulating error mechanisms

The circuit simulations are based on the schematic, shown in Fig. 2, of a 12-bit charge redistribution ADC architecture with the top five bits segmented and the remaining bits binary weighted. The architecture is split into a 7-bit main-DAC and a 5-bit sub-DAC that is capacitively coupled [2] to save area and to ease matching requirements.

When the ADC tracks the input voltage V_{in}, all the switches are as shown charging the capacitors with the input voltage. At the sampling instant the switches S_{fb} and S_{gnd} are opened, which preserves the charge on the capacitors. Then all the remaining switches are flipped, causing the comparator input voltage to go to $-V_{\text{in}}$. The SAR logic then starts a binary search for a setting of the switches at the bottom end of the capacitors for which the comparator input node returns to ground.

In the schematic, forty-one capacitors are shown, labeled with the number of unit capacitors they are made of. With all capacitors at their design values, and sufficient settling time for the comparator decision, the simulated transfer characteristic is that of an ideal ADC. The manufacturing process, however, causes the circuit elements to deviate from their design values causing the transfer characteristic to exhibit nonlinearities. As for the unit capacitors, they are expected to be mismatched stochastically; typically with a standard deviation of 0.1% of their design value.

For the example of the segment capacitors $C_{\text{seg1}},\ldots,C_{\text{seg31}}$, we show in Fig. 3 the INL characteristics simulated for the capacitors being individually increased by 0.1% of their design value. The computational costs of performing the total of 41 simulations is moderate, as the simulation time on an 800 MHz PC running MATLAB was just under one minute.

2.2. Error identification

In a manufactured device all capacitor values are mismatched simultaneously. Applying the linear superposition principle[1],

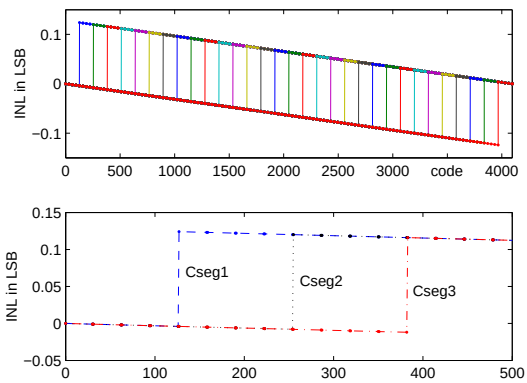

Figure 3. Simulated INL characteristics for individual segment capacitors being increased by 0.1% of their design value.

the resulting INL characteristic can be decomposed into a weighted sum of INL characteristics associated with the individual capacitor mismatches considered in the previous section.

To this end, we arrange the INL characteristics simulated for individual capacitor mismatches in a (4096×41)-matrix A with one column per error mechanism, and one row per point on the INL characteristic. We decompose a measured device characteristic $b \in \mathbb{R}^{4096}$ as

$$b = Ax + \Delta b \tag{1}$$

where x is a vector of weights, each weight associated with one of the simulated error mechanisms. The residual $\Delta b \in \mathbb{R}^{4096}$ accounts for measurement noise and the lack-of-fit of the model A. The lack-of-fit is that part of a device characteristic b that cannot be associated with one of the simulated error mechanisms.

In order to obtain a vector x of weights for the individual error mechanisms, we search for a least-squares solution of

$$b \approx Ax, \tag{2}$$

i.e. a solution x that minimizes $\|\Delta b\|_2$ in (1). Before solving (2), we estimate the rank of the matrix A. To this end, we

[1]That the linear superposition principle applies for the INL characteristic of the ADC can be assumed as the same assumption underlies linear model-based testing, which has been demonstrated successfully in a production test environment [6].

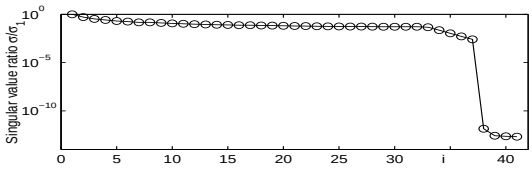

Figure 4. Plot of relative singular values σ_i/σ_1 of matrix A.

determine the Singular Value Decomposition (SVD [1])

$$A = U\Sigma V^T \tag{3}$$

and determine the rank of A based on the plot of singular values shown in Fig. 4. The sudden drop in magnitude of the singular values with index greater than 37 indicates [5] that the numerical rank of A is $r = 37$. With A being rank deficient (i.e. rank of A being smaller than the number of columns of A, that is 41) there exist infinitely many solutions to (2) that minimize the 2-norm of the residual $\|\Delta b\|_2$. Requiring, in addition, that the solution x itself has minimum 2-norm, yields a unique solution [1, Chap. 5.5]

$$x = \sum_{i=1}^{r} \frac{(u^i)^T b}{\sigma_i} v^i \tag{4}$$

where u^i denotes the i-th column of U, σ_i the i-th diagonal element of Σ and v^i the i-th column of V in (3).

2.3. Device circuit model

For 191 devices, we have collected measurements of the INL characteristic that we arrange in a (4096×191)-matrix B. The row-mean of B, denoted by $b_0 \in \mathbb{R}^{4096}$, represents the "average" device characteristic shown in the top part of Fig. 5. Applying the error identification procedure described in the previous section, we obtain the decomposition

$$b_0 = Ax_0 + \Delta b_0 \tag{5}$$

for which we plot the residual Δb_0 in the bottom part of Fig. 5. Error mechanisms other than the simulated capacitor mismatches cause the residual Δb to exhibit a characteristic shape. For incomplete settling of the comparator decision, for example, peaks of the INL characteristic at particular codes are expected.

Inspecting Δb at the codes where the most-significant bits (MSBs) are decided (that is code $2047 = 2^{11} - 1$, $3071 = 2^{11} + 2^{10} - 1$, and $1023 = 2^{10} - 1$), the residual exhibits the largest peak at code 3071, and the next largest at code 1023. Since the timing regime of the ADC design allows significantly more settling time for the MSB decision, we do not observe a peak in Δb at code 2047. However, with $\|\Delta b_0\|_2/\|b_0\|_2 \approx 8.3\%$, we infer that capacitor mismatches are the dominant error mechanisms; we address these in the following.

To obtain a circuit simulation model, we replace the design values for the capacitors shown in the schematic in Fig. 2 by capacitor values that represent the mismatches according

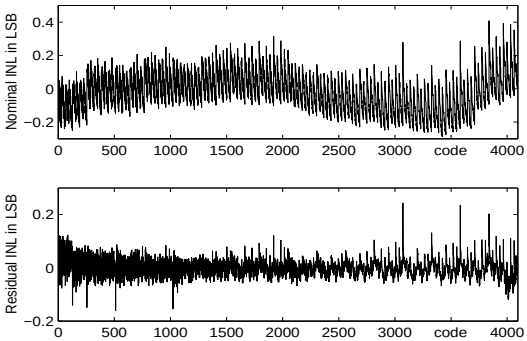

Figure 5. Average of INL characteristics measured for 191 devices (top) and lack-of-fit of simulated capacitor mismatch model (bottom).

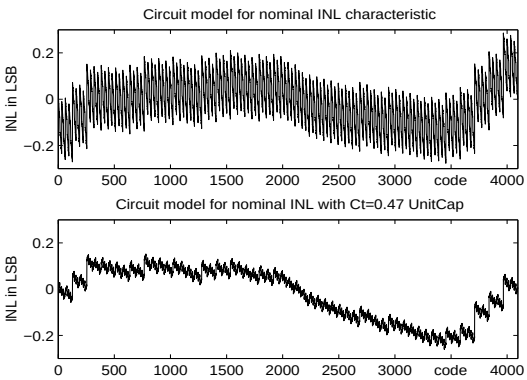

Figure 6. INL characteristic of updated ADC simulation model: identified capacitor mismatches for b_0 (top) with re-sized $C_t = 0.47$ Unit-Cap (bottom).

to the weights in x_0. For example, for C_{seg1}, whose design value is four unit capacitors, the weight in x_0 is 0.65433. This weight scales the increase of C_{seg1} by 0.1% of its design value that gave rise to the simulated INL characteristic. Thus, the updated value of this capacitor is

$$\begin{aligned} C_{\text{seg1}} &= (1 + 0.001 \times 0.65433) \times 4\,\text{Unit-Cap} \\ &= 4.0026\,\text{Unit-Cap}. \end{aligned} \tag{6}$$

Updating also the values for the other capacitors in the schematic, we obtain a circuit simulation model whose simulated INL characteristic is shown in the top part of Fig. 6, resembling the underlying shape of the INL characteristic shown in the top part of Fig. 5. With this simulation model of the ADC (which reflects the capacitor mismatches that contribute to the INL characteristic b_0) we can experiment with possible adjustments of the circuit design to reduce the INL contributions from individual parts of the circuit.

To pinpoint parts of the circuit that contribute significantly to the INL characteristic b_0, consider the decomposition we have obtained in (5). For each circuit element considered in the simulations, the INL contribution to b_0 is represented by a column in A scaled with the corresponding weight in x_0. Ranking these contributions according to their maximum magnitudes, we obtain the top-10-list of INL-contributing circuit elements shown in Fig. 7.

Addressing the largest contribution which is associated

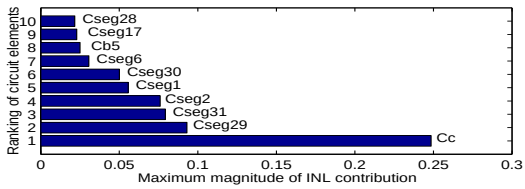

Figure 7. Top-10 list of INL contributing circuit elements.

with the coupling capacitor C_c, the weight in x_0, that is -8.14, indicates that C_c is 0.814% too small. One possibility is to increase its design value by this amount. However, insight into the device architecture suggests not that C_c is made too small, but that significant parasitic capacitance (of yet unknown magnitude) is present on the common node of the sub-DAC, labeled as C_{par} in Fig. 2. To compensate for the presence of C_{par}, we should rather decrease the design value of C_t.

By how much to decrease C_t can be determined based on the simulation model we have available. Re-sizing the termination capacitor value to $C_t = 0.47$ Unit-Cap results in a simulation model that exhibits the INL characteristic shown in the bottom part of Fig. 6. Note that halving the design value of the termination capacitor can be accomplished much easier and is more robust to process variations than increasing the design value of C_c by a small amount such as 0.814%.

Considering the next largest contributors to the INL characteristic b_0, that is the mismatch of the capacitor C_{seg29}, indicates that it is too large by 0.1% of its design value. A design change to decrease this circuit element by such a small amount does not seem feasible as process tolerances cause all the segment capacitors to be stochastically mismatched by a comparable amount. A different approach to lower the INL contributions while taking process variations into account is proposed and evaluated in the following sections.

3. Circuit reconfiguration

Reconfiguring the digital logic of a manufactured device by programming an internal EPROM or by blowing poly-silicon fuses enables the implementation of post-manufacturing calibration schemes on small geometry semiconductor processes. In this section, we consider the case where the 5-bit to 31-segment decoder is programmable during in-package test, allowing one to re-assign the capacitors $C_{seg,i}$ to individual segments with the aim of improving the linearity characteristic of the DAC and hence the ADC.

We propose a non-iterative algorithm that searches for a locally optimal reconfiguration. We give simulation results that predict a significant performance improvement for the linearity of the charge redistribution DAC. Reducing the nonlinearity of the DAC, however, will increase the relative importance of other nonlinearity contributors present in the ADC, which to address with the modeling procedures described in the previous sections would require a refinement of the simulation model to include error mechanisms other than capacitor mismatches, which, however, is beyond the scope of this paper.

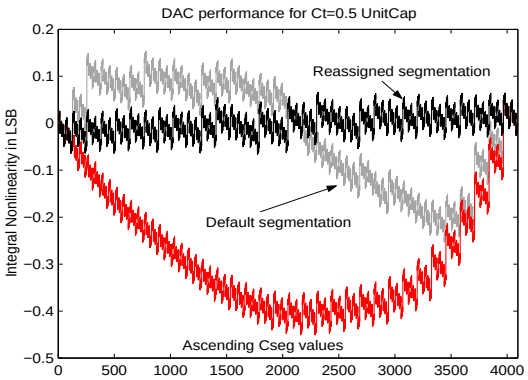

Figure 8. Simulated INL characteristic of "average" device with $C_t = 0.5$ Unit-Cap with different segment assignments.

3.1. Segment decoding

Having determined values for the 31 segment capacitors, one can revise the assignment of these capacitors to the individual segments, and thereby change the INL characteristic of a device. For example, sorting the capacitors in ascending order, assigning the smallest capacitor to C_{seg1} through to the largest to C_{seg31}, one can simulate the INL characteristic. The result for the "average" device characteristic b_0 is shown in Fig. 8. Compared to the characteristic of the default segment-to-capacitor assignment, this characteristic exhibits a significantly larger bow whose minimum value is -0.45 LSB.

Thus, when one tries to minimize the excursion of the INL characteristic, one should aim for symmetry of the characteristic. We propose to achieve this by changing the segment decoding scheme. The default decoding scheme of the five top bits, denoted by `seg5bit` to the thirty-one segment capacitor switch control lines, denoted by `segs31`, is implemented by thermometer decoding, abbreviated here as `segs31=thermometer(seg5bit)`. Changing the decoding scheme to

```
segs31= seg5bit[4]
      ? ~thermometer(31-seg5bit)
      :  thermometer(seg5bit);
```

enforces rotation symmetry around mid-scale. Note that this implementation only requires a 5-bit full-adder, a 5-bit multiplexer and 31 XOR-gates in addition to the default scheme. In the default scheme, for `seg5bit=5b'00001`, C_{seg1} is the only segment capacitor switched to V_{ref}, all the remaining are switched to ground; and for `seg5bit=5b'11110`, C_{seg31} is the only capacitor that remains switched to ground. With the changed decoding scheme, for `seg5bit=5b'11110`, C_{seg1} is switched to ground, while all the others are switched to V_{ref}.

3.2. Reassigning segment capacitors

Besides enforcing symmetry, the proposed decoding scheme always keeps the segment capacitors $C_{seg16},\ldots,C_{seg31}$ switched to the same voltage, either ground or V_{ref}, and thus,

only the mismatch of their sum contributes to the INL characteristic of the DAC. Thus, given 31 stochastically mismatched capacitors, the smallest mismatch should be "assigned" to C_{seg1}, while $C_{\text{seg2}},\ldots,C_{\text{seg15}}$ should be chosen so as to minimize the impact of capacitor mismatches on the INL characteristic.

Given a 31×31-switch-matrix that is programmable during in-package test, we can choose the assignment of each manufactured segment capacitor to the segments on the INL characteristic. In order to find the mapping that the switch matrix is to perform, we apply the circuit element identification technique used in Sec. 2.3, estimating the manufactured capacitor values from an INL measurement of a device with the default thermometer-type segment decoding. Denoting `Csegs`$=[C_{\text{seg1}},C_{\text{seg2}},\ldots C_{\text{seg31}}]$, we apply the following MATLAB function to find the required mapping:

```
1 function ind=sort_seg(Csegs);
2 Csegs=Csegs-sum(Csegs)/length(Csegs);
3 [Y,Ind]=sort(abs(Csegs));
4 ind(1)=Ind(1); Ind(1)=[];
5 for i=2:length(Csegs)
6    s=sum(Csegs(ind));
7    [Y,k]=min(abs(s+Csegs(Ind)));
8    ind(i)=Ind(k); Ind(k)=[];
9 end
```

In line 2 of the above code, the average segment capacitor value is subtracted from the value of the segment capacitors, leaving us with the mismatch for each capacitor. In lines 3 and 4, the capacitor for the first segment is chosen as the one with the smallest mismatch. However, it will cause some mismatch (denoted by `s` in line 6), and thus, some excursion of the INL characteristic, which steers the choice of the second segment capacitor in line 7.

With default segmentation and decoding, the INL characteristic of the average DAC is labeled in Fig. 8 by "Default segmentation." Reassigning the physical segment capacitors to logical segments in the manner proposed above, and changing the decoding scheme as proposed in Sec. 3.1, the resulting INL characteristic is shown in Fig. 8 and labeled as "Reassigned segmentation." As expected, the resulting INL characteristic exhibits balanced magnitudes for the maximum and minimum, and moreover, the magnitude is significantly reduced by the calibration as we chose the "best" 15 segment capacitors out of the 31 available.

3.3. Performance estimation

In order to estimate the benefits of a calibration scheme based on reassigning the segment capacitors, we consider the following DAC and ADC performance parameters:

- maximum and minimum INL, and also
- contributions of the static nonlinearity to total harmonic distortion and noise (THD+N).

For a set of 191 devices, we have measured the INL characteristics. Denoting a characteristic by $b\in\mathbb{R}^{4096}$, we perform

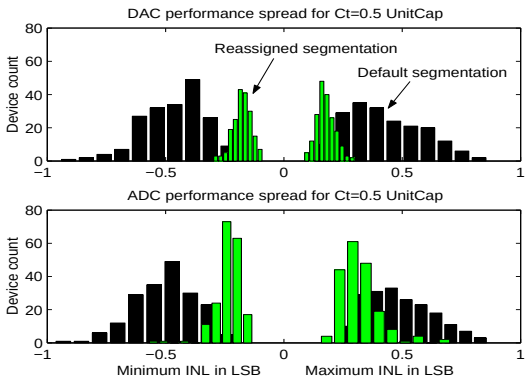

Figure 9. Histograms of maximum and minimum INL of the DAC (top) and ADC (bottom) pre- and post-calibration (black and gray bars respectively).

the decomposition (1). The circuit element values of the simulation model are obtained analog to (6). To account for the parasitic capacitance on the common node of the sub-DAC, the value determined for C_{t} is reduced by half a unit capacitor as suggested in Sec. 2.3. With this circuit model, the INL characteristic of the DAC can be simulated and is denoted by b_{DAC}.

Applying the algorithm described in Sec. 3.2 to the segment capacitor values, we obtain a new assignment of the capacitors that is implemented in the circuit simulation model by "reconnecting" the digital control signals to the switches in the DAC architecture and applying the decoding scheme proposed in Sec. 3.1. From the simulation model, we obtain the INL characteristic of the re-configured DAC, denoted by b^*_{DAC}. To determine the ADC nonlinearity of a device for a given DAC nonlinearity characteristic b_{DAC} or b^*_{DAC}, the residual Δb (accounting for non-capacitor mismatch related INL-causing mechanisms) is added at each code.

In the top part of Fig. 9, we show the histograms for the maximum and minimum element of b_{DAC} and have overlaid the histograms for b^*_{DAC}. Comparing the two histograms indicates that the DAC calibration can improve the INL performance of the devices. However, when considering the INL performance of the ADC (histograms are shown in the bottom part of Fig. 9), the improvement is offset by contributions from Δb.

The major cause of this offset is spikes in the residual characteristic Δb, which was earlier shown for the average device characteristic b_0 in the bottom part of Fig. 5. This observation indicates strongly that in order to benefit fully from improving the INL performance of the DAC, other INL-causing mechanisms have to be addressed also. In the case of the spikes at the MSB transitions, this requires an improved settling of the comparator decision, either by allocating more settling time for the MSBs or by speeding-up the dynamics of the comparator.

Another specification of the ADC is Total Harmonic Distortion and Noise (THD+N), to which the static nonlinearity of a device contributes significantly. To determine this static contribution, we use a static behavioral model of the ADC

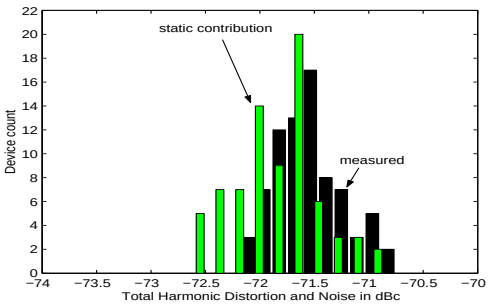

Figure 10. Histograms of measured THD+N and simulated static contribution for a set of 77 devices.

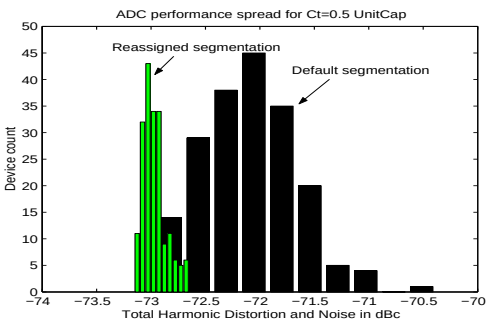

Figure 11. THD+N contribution from static nonlinearity for C_t reduced by half a unit capacitor (black) and additionally reconfigured segment capacitor sequence (gray).

with a transfer characteristic determined by a given INL characteristic. Feeding this behavioral model with a full-scale sinewave and performing an FFT of the output codes, we determine the contributions to THD+N from quantization and the static nonlinearity.

For a linear ADC, the ideal THD+N figure is -74 dBc. On the data sheet for the ADC that we use in our experiments, the specification limit on THD+N is -70dBc. For a subset of 77 devices out of the 191 devices used so far, we have additionally obtained the FFT spectrum from device measurements under dynamic conditions as stated on the data sheet. Comparing the two histograms, shown in Fig. 10, for THD+N measurements and the static contribution obtained from behavioral simulations of the ADC model with static nonlinearity indicates strongly that the static nonlinearity contribution is significant. Thus, reducing this static contribution by applying the calibration scheme to the DAC will help to improve this performance metric, but it will also prompt for improvements of the design that target dynamic error mechanisms.

In order to estimate the performance improvement obtainable by calibrating the static INL of the DAC, consider the histogram of simulated THD+N figures for the uncalibrated ADC nonlinearity $b_{\mathrm{DAC}} + \Delta b$ that is shown in Fig. 11 in black, overlaid with the histogram for the calibrated devices, i.e. $b^*_{\mathrm{DAC}} + \Delta b$, in gray. The histograms indicate a considerable performance improvement due to the calibration scheme. Note that, for THD+N, the spikes in the residual characteristic Δb have only minor contributions, so we do not show the histograms for the DAC separately.

However, it is important to notice that reducing the contributions to THD+N from the static nonlinearity is only one aspect. Other error mechanisms in the ADC that cause dynamic contributions to THD+N also have to be addressed in order to benefit fully from the calibration scheme.

4. Concluding remarks

In this work, we develop a model based on simulations of the impact of error mechanisms on the ADC's INL characteristic. This model can be inverted in order to extract (from measured INL characteristics) a circuit simulation model that reflects (the dominant part) of the error mechanisms present in manufactured devices.

These simulation models can help on the one hand to improve the design, in our case by reducing the effect of parasitic capacitances, and on the other hand to evaluate strategies to calibrate the device performance during in-package test. Opposed to traditional trimming approaches that are based on iterative "trim and measure" cycles, the model can be used to extract mismatch values for the circuit elements on the production line, and the proposed non-iterative algorithm determines the trim settings. Only a final INL measurement is required to ensure that the reconfiguration of the digital logic was successful.

Improving device performance by calibration requires one to address the dominant error sources in a given device architecture on a given manufacturing process. Evaluating different calibration strategies with the methods presented here for the example of changing the segment capacitor assignments allows one to make an informed decision on which strategy works best on a given manufacturing process. For the evaluation, an uncalibrated sample set of devices is required in addition to a simulation model of the dominant error mechanisms.

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