Selectively Clocked CMOS Logic Style

for Low-Power Noise-Immune Operations in Scaled Technologies

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Abstract

This paper proposes Selectively Clocked Logic (SCL) style based on skewed logic for noise-tolerant low-power high-performance applications. Variations of the logic style with multiple threshold voltage (MV_{th} -SCL) and multiple oxide thickness (Mt_{ox} -SCL) techniques are also studied. Simulation results indicate that SCL, MV_{th} -SCL, and Mt_{ox} -SCL circuits reduce the total power consumption (leakage plus switching power) of the ISCAS benchmark circuits by 51.5%, 53.1%, and 69.6%, respectively, with over 25% improvement in noise immunity compared to Domino circuits with comparable performance.

1. Introduction

With the demand for high performance systems, dynamic circuits, such as Domino logic, are widely used in critical paths of design. However, with continued scaling trends, it becomes more difficult to scale Domino circuits due to its low noise margin. Another problem with Domino is the high clock load since the clock is connected to every gate in the circuit and therefore, consumes a considerably large amount of power. Furthermore, all gates in Domino circuit are precharged simultaneously, increasing the peak current, peak power, and power supply noise in the circuit.

The above-mentioned problem concerning noise immunity of Domino can be mitigated by using skewed logic [1][2]. Since a skewed logic gate has the same circuit topology as a standard CMOS gate, the noise immunity is better than that of corresponding Domino gate. Due to the nature of skewed logic circuits, we can apply selective clocking scheme to selectively connect the logic gate to the clock, resulting in lower clock power consumption.

There are several ways to skew CMOS logic gates. The conventional method described in [1] and [2] changes the size of either PUN (pull-up network) or PDN (pull-down network) according to the desired transition direction. Skewed logic gate can also be achieved by changing the threshold voltage (MV_{th} -SCL) or the oxide thickness (Mt_{ox} -SCL) of the transistors in the appropriate section of the gate. These logic styles are also studied in this paper. Several ISCAS benchmark circuits are implemented with

these logic styles and compared with their Domino counterparts.

2. Skewed logic

A skewed logic gate has the same circuit topology as a classical static CMOS gate but the size of either the PUN or the PDN is increased for fast low-to-high or high-to-low transitions, respectively. Sizing the PUN or PDN to favor one transition is referred to as skewing. For example, for a fast high-to-low transition in a 2-input NAND gate, the size of the NMOS transistors in the PDN is increased. Skew is measured as the change in ratio between the PMOS and NMOS devices of the gate from its original value (i.e. W_p/W_n for equal low-to-high and high-to-low transition time).

3. Selectively Clocked Logic

In order to achieve performance comparable to Domino circuits, skewed logic circuit is operated in 2 phases: precharge and evaluation. During precharge phase, all gates are reset to their initial state through slow transition. While in evaluation phase, the circuit performs its function. To ensure the highest performance, only fast transition is allowed during evaluation phase. This can be achieved by arranging skew direction of the gates in a chain so that the gate skewed for fast high-to-low transition is followed by gate skewed for fast low-to-high transition, and vice versa. With this arrangement, precharging of gates in the chain can be propagated to the subsequent gates as long as it does not exceed the precharge phase of the clock period. As a result, not every gate in the circuit need to be connected to the clock and power consumption can be reduced. Figure 1 shows a logic block using SCL with arrows indicating the fast transition direction.



Figure 1. Logic block using SCL

Based on the concept described above, a selective clocking scheme for SCL circuits was developed. In order

to achieve the highest performance of the circuit, gates with largest skew (smallest evaluation delay) are used on the critical evaluation paths. On the other hand, to reduce the number of gates connected to the clock, we try to maximize the number of gates in each precharge chain without exceeding the precharge period of the clock. This can be done by assigning lower skew (smaller precharge delay) to gates in non-critical paths.

4. MV_{th}-SCL and Mt_{ox}-SCL

There are several ways to achieve the skewed logic characteristics besides changing the width of the transistors. Increasing the threshold voltage of transistors, either by adjusting the doping density or the body bias of the transistor, in PUN or PDN of a gate causes propagation delay in the corresponding direction to be slower due to the reduction in current drive. Increasing the threshold voltage of the transistors helps to reduce subthreshold leakage current and static power consumption.

Larger gate oxide thickness can also be used to achieve a higher threshold voltage of the transistor. However, in order to suppress short channel effect, the channel length of the transistor has to be increased to maintain a good aspect ratio [3] of the device. Changing the threshold voltage by altering the gate oxide thickness helps to reduce both subthreshold leakage and gate oxide tunneling leakage, as well as dynamic power. However, advanced process technology is required for fabricating multiple oxide thickness circuit. This type of SCL will be appropriate for technologies where gate oxide tunneling is the dominant component of leakage.

5. Results on Benchmark Circuits

Several ISCAS benchmark circuits were synthesized with different types of SCL under the Berkeley SIS environment. For simplicity, only INVERTER, 2 to 4input NAND and NOR gates with skew values of 3 to 5 were used for synthesis. For each SCL circuit, we compared its total power consumption with its Domino counterpart, which consists of 2-input AND and up to 6input OR gates, and running at the same clock frequency. A 70 nm BPTM transistor model, which is provided by the at UC Berkeley Device Group (http://wwwdevice.eecs.berkeley.edu/~ptm), with supply voltage of 0.9V was used for all simulations. The unskewed effective channel widths for PMOS and NMOS transistors were 1.5 μ m and 0.5 μ m, respectively.

Figure 2 shows the total power consumption in different ISCAS benchmark circuits implemented with different SCL and conventional Domino. The number of gates connected to clock in SCL and MV_{th} -SCL circuits are approximately 23.3% of the total number of gates, and is about 18.5% in Mt_{ox} -SCL. This results in a significant

savings in clock power. Also, applying non-alternating skew directions [4] to solve reconvergent path problem in SCL reduces the total number of gates by approximately a factor of two over Domino circuits. This reduces both circuit, as well as, clock power consumption. Moreover, the reduction in capacitance in Mt_{ox} -SCL helps in decreasing the dynamic power consumption even further. The total power of the circuits implemented in SCL, MV_{th} -SCL, and Mt_{ox} -SCL can be improved by approximately 51.5%, 53.1%, and 69.6% compared to Domino circuits, respectively.



Figure 2. Total power consumption between variations of SCL and Domino circuits

6. Conclusions

In this paper, we proposed different types of Selectively Clocked Logic (SCL). It is shown that SCL has better scalability and power consumption than Domino with comparable performance. Simulation results on ISCAS benchmark circuits indicate that SCL, MV_{th} -SCL, and Mt_{ox} -SCL circuits coupled with non-alternating skew directions can achieve approximately 51.5%, 53.1%, and 69.6% less power consumption than Domino circuits with over 25% improvement in dynamic noise immunity.

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