Techniques for Automatic On Chip Closed Loop Transfer Function Monitoring For Embedded Charge Pump Phase Locked Loops

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Abstract

Charge Pump Phase locked loops are used in a variety of applications, including on chip clock synthesis, symbol timing recovery for serial data streams, and generation of frequency agile high frequency carrier signals. In many applications PLL's are embedded into larger digital systems, in consequence, analogue test access is often limited. Test motivation is thus towards methods that can either aid digital only test of the PLL, or alternatively facilitate complete self testing of the PLL. One useful characterisation technique used by PLL designers is that of closed loop phase transfer function measurement. This test allows, an estimation of the PLL's natural frequency, damping, and 3dB bandwidth to be made from the magnitude and phase response plots. These parameters relate directly to the time domain response of the PLL and will indicate errors in the PLL circuitry. This paper provides suggestions towards test methods that use a novel maximum frequency detection technique to aid automatic measurement of the closed loop phase transfer function. In addition, techniques presented have potential for full BIST applications.

Keywords: PLL, CP-PLL, BIST, TEST, DfT.

1. Introduction

CP-PLL's (Charge Pump Phase locked loops) are used in a variety of applications including, on chip clock synthesis, bit and symbol timing recovery for serial data streams, and generation of frequency agile RF (Radio Frequency) carriers for use in FDMA (Frequency Division Multiple Access) based communications systems.

In many applications a CP-PLL is embedded into a large digital system on chip (SOC). It is also common for the PLL to be the only mixed signal component present on the SOC. In situations such as this, obviously there is a desire to use digital only test methods. In many classic tests analogue parameters are measured, thus requiring access to critical analogue nodes. This can lead to problems for embedded PLLs, in terms of both increased probability of noise injection into the loop, and limited availability of external analogue test access [1]. For many applications these problems can be eased by inclusion of on-chip test support hardware that allows conversion of the analogue PLL characteristics into a digital only format. This process can also help to integrate the PLL into a digital only design verification flow. Several recent papers [2][3][4] have investigated automated PLL test techniques.

This paper presents hardware techniques that will allow on chip monitoring of a CP-PLL's transfer function, and also allow extraction of magnitude and phase information of the response, for subsequent post processing or comparison against on chip limits. In, addition the test approach includes a novel technique to allow automatic detection of the maximum PLL output deviation. The paper is broken into the following sections:

Section 2 provides basic information relating to the measurement of the magnitude and phase response plots of a PLL. Section 3 Investigates a simple method for generation of suitable input signal for a CP-PLL transfer function test. Section 4, Investigates suitable methods for response capture and evaluation. Section 5, provides experimental and simulated results. Finally section 6, provides conclusions and indications of further work directions. Note, that throughout the paper it is assumed that the reader is familiar with aspects of CP-PLL operation. Further details of PLL operation are provided in [5] [6][7].

2. PLL phase transfer measurements.

In most applications a PLL system is designed to produce a second order system response [6]. In consequence, frequency response measurement plots of the PLL output magnitude and phase against input signal frequency are a commonly used analysis tool.

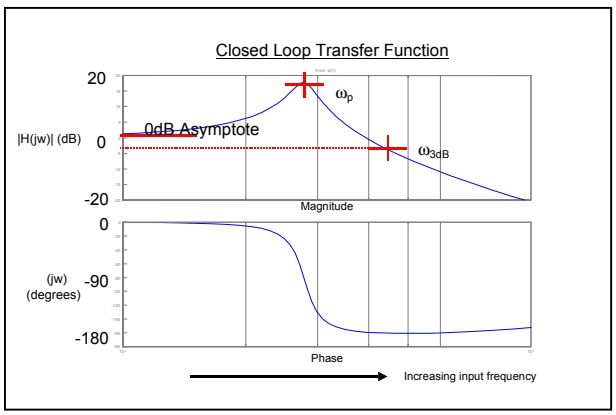

Figure 1 Phase and magnitude plots for a second order system.

For reference, typical parameters of interest of a second order system frequency response are highlighted on figure 1. These are now explained in context with a PLL system:

0dB Asymptote: For a unity gain system, as the frequency of the excitation signal is reduced below ωp, the magnitude of the gain will tend to 1 (0dB) [8]. The slope of this decrease will be determined by the damping of the system. In a similar manner the relative phase lag between the input and output of the system will tend to 0°. This fact can be used to aid test as it means that output magnitude measurements taken at a sufficiently low point below ωp can be approximated to unity gain. Additionally, the phase lag can be approximated to 0°. This means that all measurements taken from the PLL output can be referenced to the first measurement.

ωp: This is the frequency where the magnitude of the system response is at its maximum. It is directly analogous to the natural frequency (ωn) of the system. In addition, the relative magnitude of the peak (above the unity gain value can be used to determine the damping factor (ζ) of the system. Relationships between ζ, the dB Magnitude and the normalised radian frequency are available in many texts concerning Control or PLL theory [8] [9].

ω3dB: Following [6] this defines the one-sided loop bandwidth of the PLL. The PLL will generally be able to track frequency variations of the input signal that are within this bandwidth. This parameter can also be used to estimate the damping factor of the PLL [6].

It must be noted that although second order systems are considered here and a 0dB asymptote assumption is made, relative measurement of the transfer functions of higher order PLL loops will also provide valuable information about system operation, and can be achieved with the proposed methods.

Experimental extraction of the PLL transfer function using conventional techniques:

For normally encountered second order systems i.e. ones with a voltage, current or force inputs and corresponding voltage, current or displacement outputs, the frequency transfer plot is constructed by application of a sinusoidally varying input signal at different frequencies. The output of the system is then compared to the input signal to produce magnitude and phase response information. The differences encountered with a PLL system are now explained with use of the figure 2 and the associated equation (1):

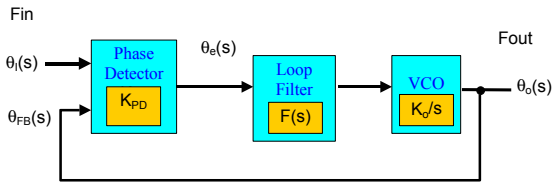

Figure 2 PLL block diagram

For the PLL systems considered here the assumption is made that the input and output signals are continuous square wave signals. The PLL's function is to phase align the input and output signals of the PLL system. Therefore with reference to figure 2 the Laplace domain transfer function of the PLL is as follows.

$$\frac{\theta_i(s)}{\theta_o(s)} = H(s) = \frac{K_{PD}K_O F(s)}{s + K_{PD}K_O F(s)} \qquad (1)$$

Where: θi and θo represent the phase of the input and output signal respectively. KPD and KO are the transfer functions of the Phase detector and the VCO (voltage controlled oscillator) respectively, and F(s) is the transfer function of the PLLs loop compensation filter.

Measurement of the PLL transfer function:

It can be seen from equation (1) and figure (2) that to experimentally measure the PLL transfer function we need to apply a sinusoidal variation of phase about the nominal phase of the input signal $\theta_i(t)$, i.e. we sinusoidally phase modulate the normal input signal. The frequency of the phase change is then increased and the output response is measured. Note that following [5] it is possible to replace phase modulation by frequency modulation. The block diagram for an experimental bench type test set-up is shown in figure 3.

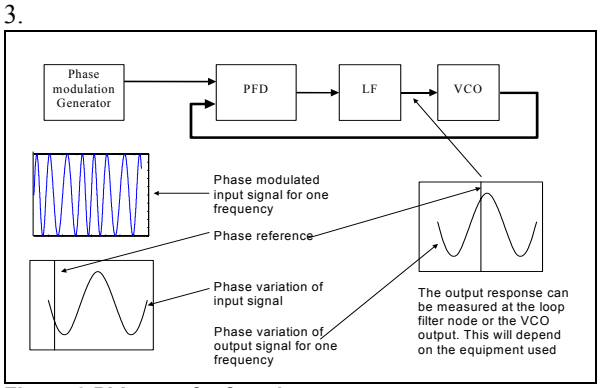

Figure 3 PLL transfer function measurement.

For the above test, the output response can be measured at the loop filter node or the VCO output. The output of the loop filter node will be a sinusoidal varying voltage and the output of the VCO will be a frequency (or phase) modulated signal. It must be noted, however, that for many systems direct access of the loop filter

node is undesirable, in consequence the tests that are explained in subsequent sections focus towards methods that access the VCO (or divided VCO) output.

3. On chip input signal generation:

When considering on chip signal generation the problem becomes how to generate a sinusoidal phase or frequency modulated input signal with the minimum of hardware overhead, and ideally using digital circuitry. This seems difficult, but fortunately, due to the filtering function of the PLL (see figure 1), a smooth input modulation is not required, and a discrete step form of input modulation can be applied whilst still producing an excellent approximation to the ideal transfer function. This can be achieved due to the fact the PLL acts as a low pass filter on the input signal.

A convenient way to generate a discrete form of frequency modulation is by use of a simple DCO (Digitally controlled oscillator). A DCO [5][6] can consist of a digital ring counter that is used to downscale a master clock signal to a set of lower frequency signals. This method can be used to produce set of discrete signals centred on a nominal frequency. Digital FM is then produced by continuously multiplexing between a set of frequencies. This method is represented in block diagram form below.

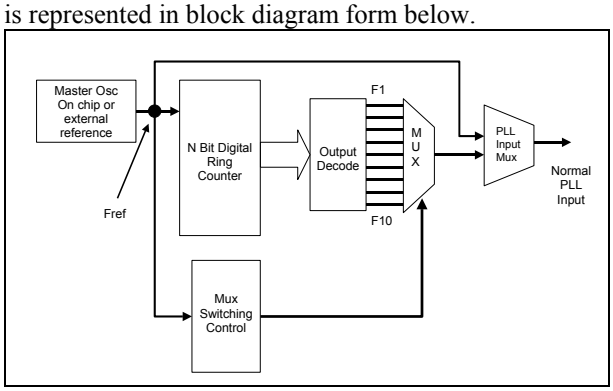

Figure 4 Discrete FM method for input signal generation.

The main problem with this method is related to the frequency resolution that can be obtained. The resolution will be determined by: The master oscillator frequency, the division ratio of the counter, and the nominal frequency of the input signal i.e.

$$\Delta F_{res} = Fin_{nom} - \frac{F_{ref} \cdot Fin_{nom}}{F_{ref} + Fin_{nom}} \qquad (2)$$

Where: ΔF_{res} is the required resolution, F_{in} is the nominal frequency of the input signal to the PLL, and F_{ref} is the frequency of the master reference oscillator.

It can be seen from the above equation that the only way to increase the resolution is decrease Fin_{nom} or increase F_{ref} .To illustrate this problem examples are provided in table 1.

Fin_{nom} (Hz)	F_{ref} (Hz)	Approximate ΔFmax required (Hz)	ΔF_{res} (Hz)
10K	10M	1K	9.99
100K	10M	1K	990

Table 1 Relationship between Fin_{nom} F_{ref} and ΔF_{res}

In table 1 ΔFmax represents the maximum frequency deviation required from the nominal frequency.

It can be seen from the table, that for the second case it would not be possible to produce any quantisation of the frequency modulation without increasing $F_{ref.}$ Despite this problem, for many applications this method could be employed. Other methods relying on tapped delay line techniques can be used for phase modulation [4][10]. However, these methods have their own specific problems related to tone resolution and response capture complexity. Use of delay line techniques in conjunction with the capture circuitry described in this paper is under further investigation.

4. Techniques for response capture.

This section briefly outlines methods that can be used for response capture and evaluation. The main point to mention with respect to response capture is that as long as it can be assured that the peak amplitude of the input phase or frequency deviation does not exceed a value that would cause the PLL components to enter a non-linear region of operation [5], accurate knowledge of the absolute magnitude of the input signal is not essential. This condition follows on from the observations made in section 2.

Before further discussion, it is essential that a brief description of the PFD (Phase Frequency Detector) is given. A CP-PLLs PFD operates only on the rising edges of its input signals. With reference to figure 2, figure 5 and the PFD section of figure 7 the basic operation is explained below.

(1) $\underline{\theta_{FB}(t) \text{ leads } \theta_i(t)}$ => LF voltage falls and VCO frequency falls to try and reduce the difference between $\theta_i(t)$ and θ_{FB} (t).

(2) $\underline{\theta_i(t) \text{ leads } \theta_{FB}(t)}$ => LF voltage rises and VCO frequency rises to try and reduce the difference between $\theta_i(t)$ and θ_{FB} (t)

(3) $\underline{\theta_i(t) \text{ coincident with } \theta_{FB}(t)}$ => The PLL is locked and in its stable state. Note: The coincident dead zone pulses of figure 5 occur due to the propagation delays in the D-type latches and AND gate.

The third point has an important test implication because it means that if the PLLs feedback path is broken and an identical signal is applied to $\theta_i(t)$ and $\theta_{FB}(t)$ simultaneously that the PLL output frequency can be held at a constant level. As explained later, this mechanism can be used to aid response capture.

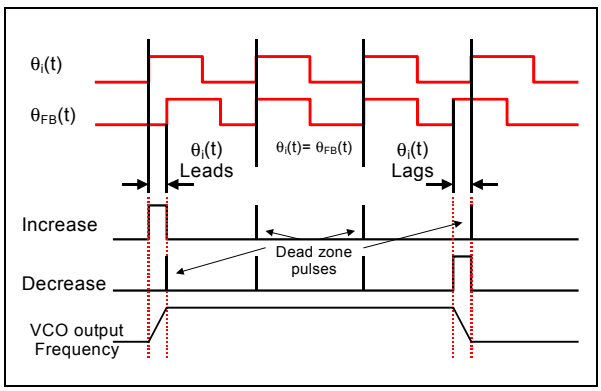

Figure 5 Graphical illustration of CP operation.

4.1. Generalised Test Hardware:

A block diagram illustrating the basic test hardware is provided in figure 6.

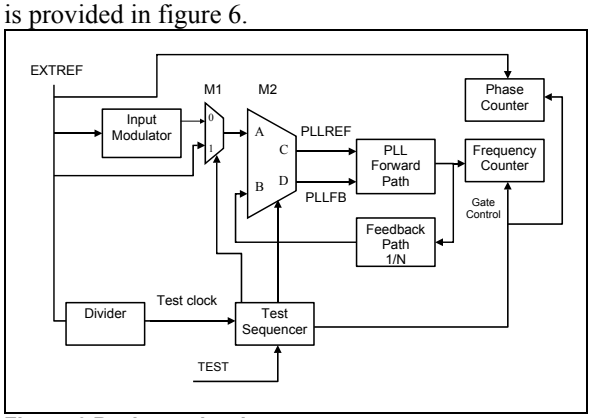

Figure 6 Basic test hardware

In figure 6 the frequency counter is used to monitor the output response. Depending on the application, the tap point for frequency measurement could be placed on the PLL output or the feedback input. The Input modulation block contains the frequency multiplexer and control circuitry to determine the input modulation frequency (see figure 4). Use of the blocks is explained in table 2. The explanation is given for a single input frequency and assumes that the PLL is initially locked.

Test Stage	M1	M2		Comments
(1) Ref set	0	A=C	B=D	Apply digital modulation with frequency **FN** Start Phase counter (counter referenced to EXTREF)
(2) Set Phase counter	0	A=C	B=D	Start phase counter at peak of input modulation
(2) Monitor Peak	0	A=C	B=D	Monitor for peak output signal frequency
(3) Peak occurred Lock PLL stop Phase counter	X	A=C	A=D	Holds the output frequency constant.
(4) Measure frequency and phase	X	A=C	A=D	Count output frequency and store. Store the result of the phase counter.
(5) Increase Modulation Frequency **FN** and repeat steps 1 to 4 until all frequencies of interest have been monitored.				

Table 2 Basic test sequence.

4.2. Output monitoring and response evaluation:

To measure the transfer function of the PLL we need to be able to at the least.

- Detect the peak of the output signal and its relative magnitude with respect to a measurement made well within the loop bandwidth.
- Detect the time difference between the occurrence of the peak of the output signal and that of the input signal.

The above processes will facilitate measurement of the PLLs magnitude and phase response, respectively.

An interesting and novel method for detecting the peak output frequency of the PLL is to use a peak frequency detecting circuit that generates an output pulse at the peak frequency of the PLL output waveform. Then, to facilitate measurement of the peak output frequency, the output pulse can be used to trigger hold circuitry (see table 2 and figure 6). For a sinusoidal variation in input frequency, the existing PFD in the PLL can, after undergoing slight modification, be used to perform a peak detecting function. This is illustrated in figure 7.

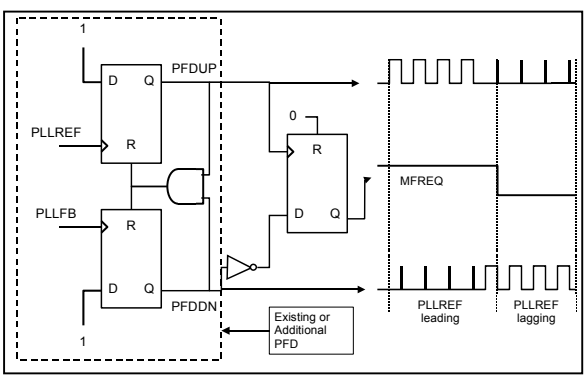

Figure 7 Sampling of output frequency

Note that in figure 7, the circuitry is set up so that when PFDDN is predominantly on (PLLREF lagging), the sampling D-latch always sees a 0 on its input. This is achieved by use of the inverter, which delays and inverts the PFDDN signal, so that the glitch pulse will not cause incorrect sampling. It can be seen that the circuitry is clocked from the dead zone glitches during part of its cycle, which is not a generally recommended design practice, however, in the particular application (see section 5) the circuitry operates correctly. If clocking is a problem, the dead zone glitches can be widened to usable signals by placing additional delay elements between the PFDUP and PFDDN outputs and the AND gate inputs. Additionally, it must be noted that the detection circuitry should be designed so that it does not impair PLL operation. In consequence, the preferred method is to construct an additional PFD specifically for the purpose of monitoring the feedback and reference signals (see figure 7 and section 5).

The output waveforms for the circuit taken from simulations are shown in figure 8.

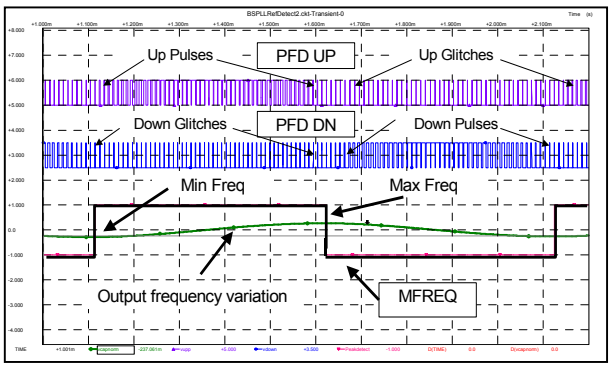

Figure 8 Sampling of output frequency

Note that in the waveforms depicted in figure 8, the output variation was monitored at the loop filter node.

5. Experimental results.

Experimental verification of the test was carried using an ATMEL AT40K20 FPGA in conjunction with a 74HCT4046AN CP-PLL [11]. The feedback dividers, reference dividers and test circuitry were implemented on the FPGA. The on chip test stimulus was created using the DCO technique and the peak frequency was detected using the modified PFD approach explained in section 4. The PFD circuitry used for response capture was constructed on the FPGA. To minimise effects of delays in the critical signal paths, where possible, adjacent macro cells and I/O pins were used in the FPGA design [12]. The loop filter (F(s)) configuration used for the PLL is illustrated in figure 9.

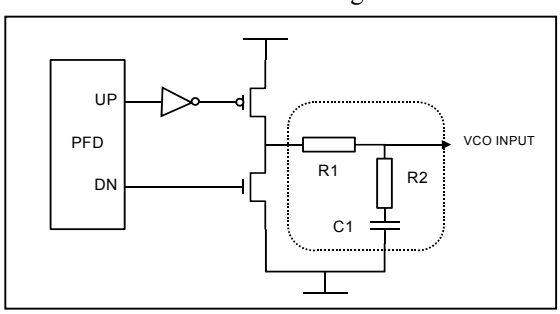

Figure 9 Loop filter configuration.

The transfer function for the filter circuitry is

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \qquad (3)$$

Where: τ_1 = R1C1 and τ_2 = R2C2

Substituting (3) and the N divider ratio (see table 3) into (1) and rearranging yields.

$$\frac{\theta_o(s)}{\theta_i(s)} = H(s) = \frac{NK_{PD}K_O(s\tau_2 + 1)}{s^2 N\tau_1 + sK_O K_{PD}\tau_2 + K_O K_{PD}} \qquad (4)$$

The calculated PLL parameters and other pertinent test information are provided in table 3.

Parameter	Value
PLL reference nominal frequency	100KHz
Maximum frequency deviation of reference signal.	1KHz
Number of discrete FM steps used	10
FM reference frequency	100MHz
Ko -> VCO gain.	2 Mrad/s/v 318.3 KHz/v
Kpd -> Phase Detector gain.	0.4V/rad
N	25
R1 (see figure9)	2.2KΩ
R2 ""	330Ω
C1 ""	470nF
Natural Frequency ωn	5187.6 r/s 825.63 Hz
Damping ζ	0.4023

Table 3 Parameters for the test set-up

Where ωn and ζ were calculated using the following relationships.

$$\omega_n = \sqrt{\frac{K_O K_{PD}}{N(\tau_1 + \tau_2)}} \quad \text{(r/s)} \qquad (5)$$

$$\zeta = \frac{\omega_n \tau_2}{2} \qquad (6)$$

The theoretical plots for the PLL system based on equation 4 are shown in figure 10.

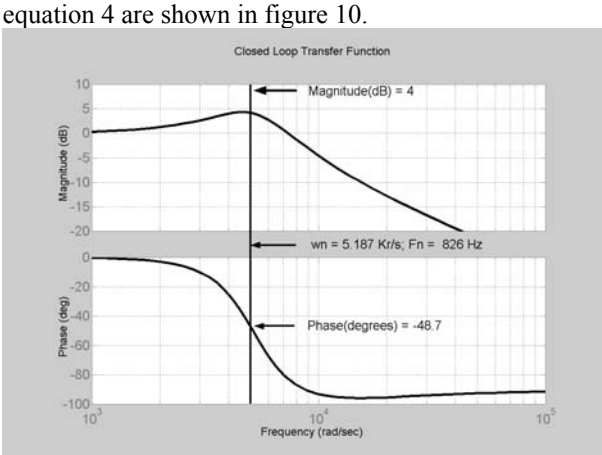

Figure 10 Theoretical magnitude and phase plots.

Experimental measurement of the real PLL system was carried out in the following manner:

The magnitude response was calculated using the relationship.

$$A_F = 20\log\frac{\Delta F\,\max}{\Delta Fref\,\max} \qquad (7)$$

Where: Af is the gain measurement taken at a particular excitation frequency, ΔFmax is the maximum deviation of the output signal, and ΔFrefmax is the maximum frequency deviation of the output signal within the loop bandwidth (excluding the region around the Natural frequency).

The frequency response was calculated by counting pulses from the occurrence of the peak magnitude of the input signal to the peak magnitude of the output signal, and then using the following relationship to give the phase delay in degrees.

$$PhaseDelay = \frac{T \bmod}{\Delta TN} \cdot 360 \quad \text{(degrees)} \qquad (8)$$

Where: Tmod is the period of the modulation frequency, ΔT is the period of the test clock, and N is the number of pulses that occur between the maximum input and output deviations.

Figures 11 and 12 show the magnitude and phase response plots taken from measured results.

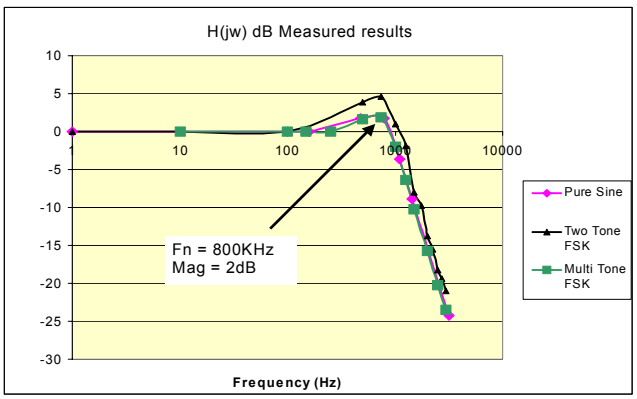

Figure 11 Measured magnitude response results.

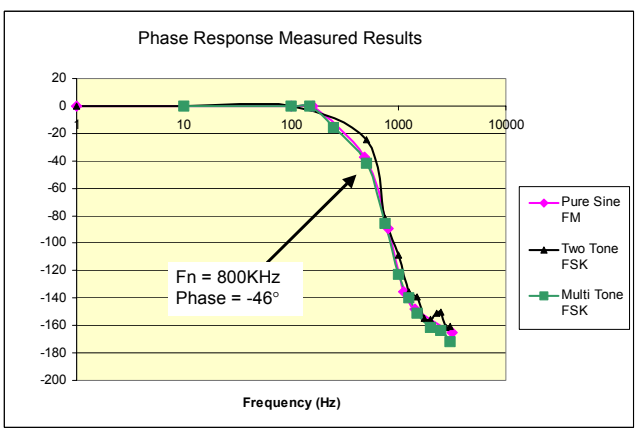

Figure 12 Measured phase response results.

For the plots shown in figures 11 and 12, measurements were taken using pure sinusoidal frequency modulation and Multi tone FSK with ten steps about the nominal frequency. In addition, a comparison is shown for a two tone FSK input signal. It can be seen from the response plots that the ideal sinusoidal FM plot closely corresponds to the ten-step FSK plot. In addition, it can be seen that the measured results match quite closely to the theoretical results shown in figure 10. The discrepancy between theory and measured results can be accounted primarily to the non-linear operation of the particular charge pump and loop filter configuration.

6. Conclusion

This paper has presented techniques that are applicable to automatic on-chip monitoring of the closed loop transfer function of a CP-PLL. In addition, a novel technique has been presented that allows the peak output frequency deviation of the PLL to be captured automatically. This technique has the potential to overcome problems encountered with estimation of the peak output response. Furthermore, the tests require no access to critical PLL nodes. Output results from the test were shown and they compare closely to an ideal analytical response curve. The main draw back of the approach shown relates to the high reference frequency required for the DCO input. Other techniques are available for generation of this signal and currently research is being carried out into development of hybrid DCO, Delay line and delay locked loop generation techniques.

Acknowledgement

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References

[1] M. Burbidge, A Richardson, A Lechner, "Test Techniques for Embedded Charge Pump PLL's; Problems, Current BIST Techniques, and Alternative Suggestions." 7th IEEE International Mixed Signal Test Workshop, June 13th-15th, 2001

[2] S. Sunter & A. Roy: 'BIST for Phase-Locked Loops in Digital Applications', IEEE International Test Conference, 28-30th Sept. 1999, Atlantic City, NJ, USA, pp 532-540

[3] S. Kim & M. Soma, 'An Effective Defect-Oriented BIST Architecture for High-Speed Phase-Locked Loops' ,IEEE VLSI Test Symposium, 30th. April - 4th May 2000, Montreal, Canada, pp 231-236

[4] B. R. Veillette, G. W. Roberts, "On-Chip measurement of the jitter transfer function of charge pump phase locked loops" Proc. Int. Test Conf, 1997, pp 776-85

[5] R Best, "Phase Locked Loops, Design Simulation and Applications", 4th Edition, Mc-Graw-Hill, ISBN 0071349030

[6] F M Gardner, "Phase lock Techniques"; Second edition; Wiley Interscience; 1979.

[7] B Razavi (Editor), "Monolithic Phase-Locked Loops and Clock Recovery Circuits; Theory and Design", IEEE Press 1996, ISBN 0780311493.

[8] J Schwarzenbach, K.F. Gill, "System Modeling and Control", Third edition, Edward Arnold, 1992, ISBN 034054379

[9] Paul H Young; "Electronic Communications Techniques"; Third edition; 1994; pp 411-423.

[10] G A S Machado (Editor), "Low Power HF Microelectronics a Unified Approach", IEE Circuits and Systems Press, 1996, ISBN 0852968744

[11] 74HC/HCT4046A Phase-locked loop with VCO, Philips Semiconductors Data Sheet, November 1997.

[12] M J Burbidge, A. Richardson, F. Poullet, J. Tijou "Investigations For Minimum Invasion Digital Only Built In "Ramp" Based Test Techniques For Charge Pump PLL's", Proc 7th IEEE European Test Workshop, May 26th-29th 2002.