An Industrial/Academic Configurable System-on-Chip Project (CSoC): Coarse-grain XPP-/Leon-based Architecture Integration

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Extended Abstract

This paper describes the actual status and results of a dynamically Configurable System-on-Chip (CSoC) integration, consisting of a SPARC-compatible LEON processor-core, a commercial coarse-grain XPP-array of suitable size from PACT Informationstechnologie AG, and application-tailored global/local memory topology with efficient Amba-based communication interfaces. The given adaptive architecture is synthesized within an industrial/academic SoC project onto 0.18 and 0.13 µm UMC CMOS technologies at Universitaet Karlsruhe (TH). Due to exponential increasing CMOS mask costs, essential aspects for the industry are now adaptivity of SoCs, which can be realized by integrating reconfigurable re-usable hardware parts on different granularities into Configurable Systems-on-Chip (CSoCs) [1].

PACT´s XPP architecture realizes a new runtime re-configurable data processing technology that replaces the concept of instruction sequencing by configuration sequencing with high performance application areas envisioned from embedded signal processing to co-processing in different DSP-like application environments. The adaptive reconfigurable data processing architecture consist of following components (figure 1):

- Processing Array Elements (PAEs), organized as Processing Arrays (PAs),
- a packet oriented communication network,
- a Configuration Manager (CM) tree, and
- a set of I/O modules.

The basic concept consists of replacing the Von-Neumann instruction stream by automatic configuration sequencing and by processing data streams instead of single machine words, similar to [2]. This supports the execution of multiple data flow applications running in parallel. A PA together with one low level CM is referred as PAC (Processing Array Cluster). The low level CM is responsible for writing configuration data into the configurable objects of the PA. The here implemented CSoC architecture (figure 1) consists of a PAC XPP-core with 32-bit datapaths, a RISC LEON µcontroller, and three SRAM memory modules. The size of the XPP architecture is 16 ALU-PAEs, a 4x4-array, and 8 RAM-PAEs. The selected and implemented communication structure is a AMBA-based multilayer AHB [6]. The XPP architecture has four IO-interfaces for input and output directed streams. We designed an AHB-bridge which connects each IO-interface of the XPP separately to the multilayer AHB. Due to the fact, that the AHB concept is based an the master/slave communication, we chose an unusual method and combine two ports, one master and one slave port as a dual port in the same bridge. This combination allows us to be flexible enough to process various application scenarios. In this way the XPP architecture is able to handle the data from a RAM-module or gets a stream from another master on the CSoC. The CM unit implements a separately memory for faster storing and loading the XPP configurations. If there isn't enough memory space for storing the configurations in local XPP memories, it is possible to use the global CSoC memory banks. The AHB-bridge for CM will be a single ported AHB-slave-bridge.

The LEON VHDL model implements a 32-bit processor compatible to the SPARC V8 architecture. It is designed for embedded applications with following features: separate instruction and data caches, hardware multiplier and divider, interrupt controller, two 24-bit timers, two UARTs, power-down function, watchdog, 16-bit I/O port and a flexible memory controller. Additional modules can easily be added using the on-chip AMBA AHB/APB buses. The LEON core acts as a master on this CSoC architecture. First area results by using UMC 0.13 µm technology LEON processor needs 0.7sqmm and could be clocked up to 300 Mhz, if needed (see figure 1).

The bandwidth of the AHB interface operating at 100 Mhz and 32 bit is 400 MBytes/sec, which is sufficient for future

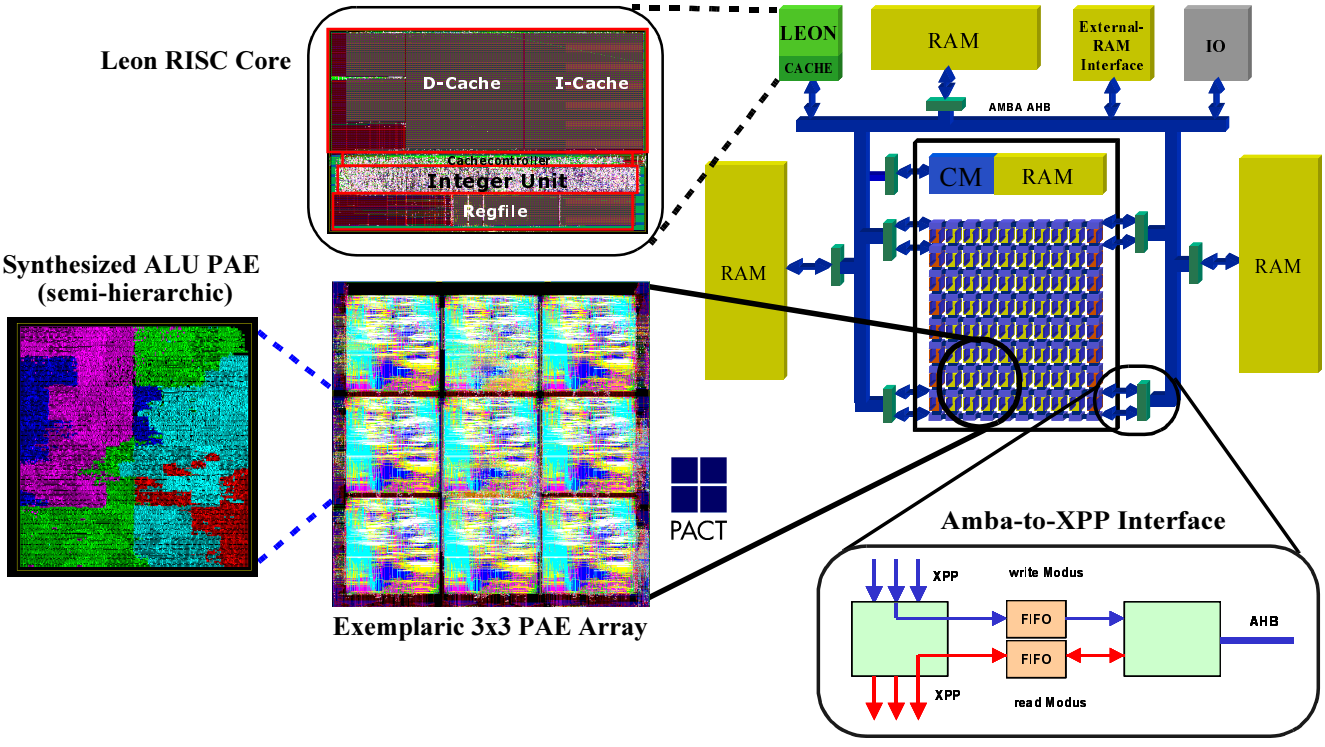

Figure 1: XPP-/LEON-based CSoC Architecture with Multi-Layer Amba-Interface

multimedia and wireless applications to supply the XPP-architecture with data and configurations and to handle the program data of the LEON efficiently. The interfaces of the memory modules to the AHB are operating in slave modus, whereas single arbiters and multiplexers are used per slave to choice the right master for communication. In this way, the bus is splitted in several sub-busses allowing simultaneous transactions between various masters and slaves..Additionally, there will be an external RAM interface implemented, which allows to connect external memory to the CSoC. The communication between the CSoC and the outside world can be realized through a master/ slave AHB/PCI host bridge. The AHB master ability admits direct transfers from PCI to internal RAM without involvement of the LEON µcontroller. Otherwise, the slave ability admits the transfers between all masters and the PCI-Bridge on the CSoC. The three SRAM memory modules provide up to 3 MB on-chip. The complete size is splitted into 2x1,2 MB and 1x0,6 MB modules. The decision about the memory dimensions is based on analyzed MPEG-4 application tailored scenario, which needs the memory space for storing of two pictures and program code with XPP configurations.

The adaptivity and multi-purpose usability of CSoCs promises an attractive potential for embedded system industry in different application areas, e.g. (wireless) communication (-> multi-standard, different bandwidth and services), automotive (multi-purpose architecture platforms for all kind of control and multimedia in cars), etc.

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