LIT - An Automatic Layout Generation Tool for Trapezoidal Association of Transistors for Basic Analog Building Blocks

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Abstract

This paper describes a methodology for analog layout synthesis based on the automatic generation of an equivalent composite transistor with the same DC current characteristics of the transistors in the electrical schematic. The tool serves a dual purpose: i) the layout synthesis of analog blocks over a digital sea-of-gates pre-diffused array, and ii) the generation of custom associations of transistors for matched common-source input pairs and current mirrors. The LIT tool generates the layout in a line-matrix, sea-of-gates with gate isolation style of several blocks: the trapezoidal-like composite transistors and of matched transistor pairs. In addition, the tools provides an environment for manual analog cells placement and automatic routing. These features drastically reduce the design time, reduce costs and include matching properties.

1. Introduction

Full custom integrated circuit design methodologies require a complete process cycle. Fabrication can take four or more weeks and may delay substantially the introduction of a new product in the market. Additionally, a dedicated process run is expensive, and economic factors must determine if this alternative is viable. Other alternative is to use pre-diffused arrays, which have the advantage to incur in lower non-recurrent costs and, thus, are more attractive for small-scale production. In this strategy, wafer lots containing primitive cells of transistor arrays are manufactured by vendors and stocked. All the front-end fabrication steps are finished before customization. The metal interconnections, vias, and passivation need to be fabricated to produce the chips. These layers are designed and applied to the pre-fabricated wafers, reducing the turn-around time to a week or a few days for direct-write lithography. The sea-of-transistors (SOT) pre-diffused arrays were initially developed solely for digital circuits. Nowadays FPGAs dominate the market for fast prototyping, since they provide both multi-million gates design and a powerful and inexpensive CAD environment for automatic synthesis and technology mapping. The trapezoidal association of transistors technique (TAT) [1] appeared as an alternative way for designing analog circuits over a pre-diffused array. Hence, for mixed-mode analog-digital circuit design, the pre-diffused array can offer an alternative for semi-custom, while the FPGA architecture provides exclusively digital functionality.

2. The LIT Tool

LIT is a tool for analog circuit design that combines TAT technique and sea-of-transistors methodology in the same environment and provides automatic layout generation. It can be used as a module generator, even if pre-diffused SOT array is not used. For mapping the analog designs into the array, each transistor from the initial design is translated into one equivalent trapezoidal association of transistors (TAT). This association was proposed in [1] and is formed by identical unit-size transistors. Fig. 1 shows the TAT association schematic. MD is the equivalent top transistor and MS is the equivalent bottom transistor. Let ND be the number of unit-size transistors in parallel that form MD and NS the number of unit-transistors that form MS, then the equivalent aspect ratio may be approximated by a linear conductance association, such that

$$\left(\frac{W}{L}\right)_{Eq} = \frac{ND \cdot NS}{ND + NS} \cdot \frac{W_{UN}}{L_{UN}} \qquad \text{(eq. 1)}$$

Several different possible pairs (ND,NS) do exist for the same $(W/L)_{Eq}$. The LIT tool provides to the user a table containing all these possible values. The best choice is not obvious, since the designer has to trade-off the minimization of the parasitic capacitance and the reduction of the output conductance of the TAT association. At this stage the circuit designer has to choose and pick one of the associations suggested by LIT. After the conversion of each single-transistor on an equivalent

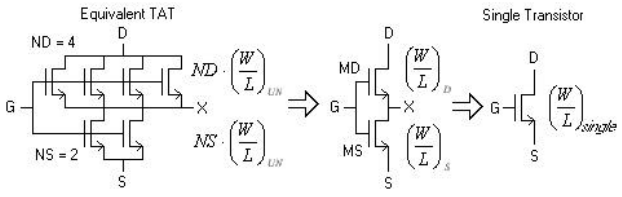

Fig. 1 - Single transistor and TAT equivalent.

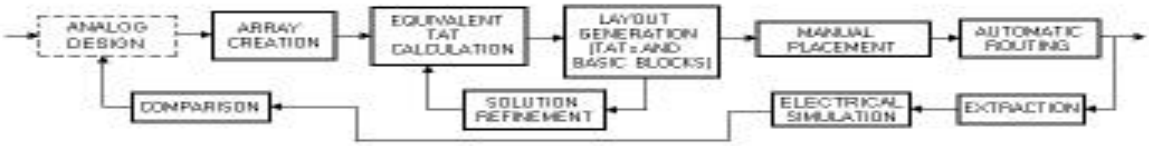

Fig. 2 - LIT design flow

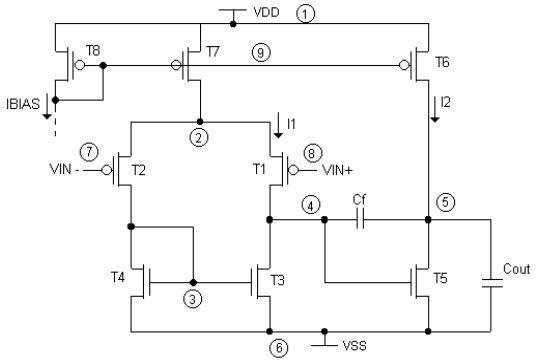

Fig. 3 - Miller amplifier schematic.

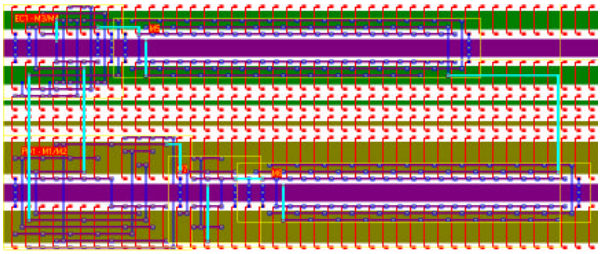

Fig. 4 - TAT Miller amplifier layout (capacitor C_f not shown)

TAT, the overall goal is that the LIT generated circuit must have similar performance to the full-custom specifications. The design flow is indicated in fig. 2. The LIT tool supports the forward path (from array creation to automatic routing) for the analog design. Next we deal with specific capabilities of LIT to generate the layout of transistor modules, transistor pairs, current sources, etc.

A complete analog circuit in general is designed from a smaller set of basic blocks that can be modeled individually: current mirrors, differential pairs, current sources, etc. The LIT tool in its current version implements the layout of four blocks: differential input pairs, current mirrors, capacitors and TAT associations that emulate a single transistor. Differential pairs and current mirrors are synthesized individually due to their matching requirements. Layout techniques are observed by LIT to improve matching, according to basic matching rules.

The LIT tool has the flexibility to generate user-specified line matrixes of arbitrary diffusion widths. Hence, the layout generator can be used for full-custom block generation that follows the TAT association methods. In this case, a pre-diffused SOT is not assumed as a constraint to the layout methodology; rather, LIT is used as a specific analog cell generator with interesting built-in matching capabilities.

3. Design Example Using the Proposed Flow and LIT Tool

In order to test the proposed design methodology, the design of a two-stage Miller amplifier in a 0.35µm digital technology is shown. This circuit exemplifies the application of the basic analog cells with layouts generated by the LIT tool. The schematic of the Miller amplifier can be seen in Fig. 3. We can divide this circuit into four different basic blocks: differential pair (T1/T2), 2 current mirrors (T3/T4 and T6/T7/T8), single transistor (T5) and a feedback capacitor (Cf). The synthesis was done with LIT tool, and the generated layout (Fig. 4) was extracted. The final performance of the TAT design with all-mininum L was compared to the original single-transistor design, resulting in similar GBW, same dissipation and slew-rate, and less DC-gain for the TAT version of the Miller amp.

4. Conclusion

LIT is a tool dedicated to analog integrated circuit design over a pre-diffused transistor array using the trapezoidal association of transistors technique. The tool automates the most common analog blocks (differential input pairs and current sources). On-the-fly generation of more complex circuits is done. These features reduce the design and prototyping times for analog integrated circuits in the same chip of the SOT digital modules. The intent of LIT is to provide a useful tool even for non-expert analog designers in a mixed-signal CMOS circuit.

References

[1] Gallup-Montoro, C., Schneider, M., Loss, I.; Series-Parallel Association of FET's for High Gain and High Frequency Applications; In: *IEEE JSSC*, Vol 29, No 9, Sep, 1994.

[2] Aita, A. L., Parisoto, A. M., Bampi, S.; Sea-of-Transistors (SOT) Array Dedicated to Analog-Digital Circuit Design; In: *Proc. SBCCI Symp.*; Sep. 1996; pp. 238-246.

[3] Choi, J. H., Bampi, S.; OTA Amplifiers Design on Digital Sea-of-Transistors Array; In: *Design, Automation and Test in Europe 1999 - DATE'99*; Germany; March 1999.

[4] Choi, Jung H.; *Mixed-Signal Design of Sigma-Delta Modulators on the Pre-Diffused Array Using Trapezoidal Association of Transistors*; Ph.D. Thesis, UFRGS Univ.; August 2001