Embedded software in digital AM-FM chipset

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Abstract

The new standard DRM for digital radio broadcast in AM band requires integrated devices for radio receivers at low cost and very low power consumption. A chipset is currently designed based upon an ARM9 multi-cores architecture. This paper introduces the application itself, the HW architecture of the SoC and the SW architecture which includes physical layer, receiver management, the application layer and the global scheduler based on a real-time OS. Then, the paper presents the HW/SW partitioning and SW breakdown between the various processing cores. The methodology used in the project to develop, to validate and to integrate the SW covering various methods such as simulation, emulation and covalidation is described. Key points and critical issues are also addressed.

One of the challenge is to integrate the whole receiver in the mono-chip with respect to the real-time constraints linked to the audio services.

1. DRM Application

DRM (Digital Radio Mondial) is a new standard promoted by the major broadcasters and receivers manufacturers. The physical layer is based upon an OFDM modulation and includes multiple configurations (channel width, code rate, protection, ...) to cope with various propagation schemes. The service layers are mainly composed by enhanced MP3 audio decoder and data services. The standard introduces also complementary services like Automatic Frequency Switching (AFS). The signal processing reference requires about 500Mips to handle the whole treatment.

2. DIAM SoC Architecture

A full software implementation will not meet the specific constraints of the radio receivers in term of die size and of power consumption. The first step is the HW/SW partitioning based upon the existing software. Profiling tools have been used to extract the memory and the CPU requirements for each sub function. Dedicated modules have been identified as candidate for a wired

implementation. Viterbi decoder including de-puncturing and digital down conversion (Wide band conversion) have been selected.

The remaining CPU requirements decrease then below 200Mips which are achievable using state of the art technology. Due to the characteristics of the channel coder, standard embedded DSP processor are not compatible with the addressing requirements. The selected solution is based on two ARM9 core plug on a multi-layer AHB matrix.

The challenge is then to size the architecture in term of CPU, memory but also the throughput according to the targeted algorithms. For this purpose, simulation tools from ARM has been used (ADS 1.2). However, the simulation does not take into account the impact of the cache, of the tightly coupled memory and the impact of the communication network. Margin has been set to avoid any real-time issue with the first version of the plat-form. For flexibility purpose, each resources are visible by each core but no arbiter has been integrated within the chip. The software has to manage this constraint and to allocate properly each resource. This flexible approach allows to change the software repartition when required.

The following figure presents an overview of the platform architecture of the DIAM base band.



Figure 1. Architecture of DIAM base band

The first version of the platform is processed in an ATMEL CMOS 0.18µm technology.

3. SW architecture

Basically, the software has been split according to the data flow and the available CPU. The physical layer has been mapped to one core and the application layers are mapped onto the second core. Cache and TCM size have been tuned to the specific requirements of the most demanding function. TCM are assigned to the audio coder which presents the strongest constraint regarding the real-time.

The figure below presents an overview of the software architecture.



Figure 2. SW architecture of DIAM base band

The platform boot is not shown although its definition is quite tricky. Indeed, without any precaution both cores will execute the same code. The retained solution for the DIAM platform is based upon remap technique which allows to translate the base of the second core.

4. Software integration

The challenge of the development is the concurrency of the HW design and the SW coding. Main issues are related to SW validation without the final plat-form and on the other hand to assess the performances of the architecture. To manage this issue, an heterogeneous strategy has been set-up.

The low level SW (drivers) has been jointly developed by the HW and SW team. As they are closely linked to the plat form their validation has been performed using VHDL/Verilog simulation including a C model for the cores.

For the upper layer, a standard approach has been adopted with the exception of the MLC. Basic modules have been identified and optimised directly in ASM instead of C approach to obtain a library. This library has been validated using the ARM tools (ADS V1.2) and reference patterns provided by the signal processing algorithm. Then, the application is developed using the critical functions of the library. The results are validated using the Integrator board from ARM.

The MLC coding scheme is implemented in HW and SW. Due to the complexity and the flexibility of the MLC a complete simulation is not achievable. A prototype on Excalibur platform from Altera has been developed. The Viterbi decoder with the de-puncturing model has been integrated in the PLD part of the devices and the SW has been mapped onto the ARM9 core. 36 sequences have been used to obtain a sufficient validation coverage. These tests highlight one mismatch between the real implementation and the bit true model on the post processing metrics engine. The prototyping board allows to run the complete validation plan in less than 1H instead of 300H using classical UNIX model.

Previous steps perform unitary validation without any exchange between SW modules. The next challenge is to validate the global software covering exchanges, memory mapping strategy, cache strategy, signalling protocol and the global performances. The foreseen solution is to develop a prototyping board integrating the 2 cores and the relevant modules. Alternative solution as Seamless has been investigated but the execution time is too slow regarding the minimum set of simulation to be done (at least few seconds). This validation will be the next step of our design.

5. Conclusions

The methodology applied during this HW/SW co-design allows us to cover efficiently the platform requirements. Several remaining points are still open and will be validated during the integration phase directly on the physical platform. However, all the open points are related to the SW and do not impact the HW.