

# Tutorials

## **A1 System Level Specification Beyond RTL**

Organizer: Daniel D Gajski, UC Irvine, US  
Speakers: Jianwen Zhu, Toronto U, CAN  
Ahmed Jerraya, TIMA, Grenoble, FR  
Andreas Gerstlauer, UC Irvine, US  
Daniel D Gajski, UC Irvine, US

Complexities of present systems or SoC designs are forcing the movement to a higher level of abstraction than RTL. With most of the system containing a large portion of software, the present languages, methodologies and tools are not adequate to tackle system-level design.

The movement to programming languages or extensions of programming languages seems to be in the right direction. In this tutorial we will discuss the basic models of computation and requirements for specifying software, hardware and complete systems. Furthermore we will give an overview of available languages, methods and models. Then, we will discuss some experiments in describing systems with presently leading system level languages such as SystemC and SpecC.

Finally, we will give an overview of other specification efforts, discuss the essential issues surrounding system-level design specification, synthesis and verification, and forecast future trends in system-level design flows.

## **B1 Low Power/Low Energy Embedded Software**

Organizer: Peter Marwedel, Dortmund U, DE  
Speakers: Peter Marwedel, Dortmund U, DE  
Luca Benini, Bologna U, IT

With a focus on programmable embedded systems, this tutorial will:

- survey the interaction of architecture, operating systems, compilers and memories from a power/energy focus
- present specific contributions of each part to power and energy, and
- outline software techniques for minimisation of power/energy.

In the first section, an introduction to the topic will be provided. Due to the large influence of the memory architecture on the total energy consumption, different memory architectures will be presented next. We will show how partitioned memories can help reducing the energy consumption.

In the next section, we will describe how partitioned memory architectures and other features of embedded systems can be exploited in compilers. This includes the exploitation of caches. In addition, this includes an analysis of the size of register files. Furthermore, we will explain techniques for reducing the memory traffic by global optimisations designed for multimedia applications. This section also comprises a description of applicable standard compiler optimisations and their potential for energy reductions as well as a brief introduction to compression techniques.

The final section describes system software and real-time operating system (RTOS) issues. This will include hardware for RTOS-based power management, software support for power management, power-aware process scheduling and power-aware device management. Exploitation of application-specific information and power management of distributed systems will also be covered.

## **C1 Test Resource Partitioning Strategies for SoC**

Organizer: Yervant Zorian, LogicVision, US  
Speakers: Yervant Zorian, LogicVision, US  
Michael Rodgers, Intel, US

The 2001 ITRS Roadmaps have been expanded to address more of the test cost challenges that impact SoC design and manufacturing test processes. In the area of test challenges, System-on-Chip (SoC) designs are included in the test chapter for the first time. In addition, new trends in manufacturing test resources are covered for the first time. This tutorial sheds light on the SoC test requirements in terms of embedded and external test resources. It analyses several challenges described in ITRS 2001 roadmaps, and presents strategies to adopt in order to address these challenges. The tutorial concentrates on the on-chip trade-offs, centralised and distributed test resources, and their scheduling solutions. It also discusses the off-chip test resources and their partitioning between hardware and software. The tutorial concludes by looking into future SoC trends and the corresponding test resource partitioning (TRP) needs.

This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2002

## **E1 Design Methodologies and CAD Tools for Mixed-Signal and RF ICs**

Organizer: Georges Gielen, KU Leuven, BE  
Speakers: Georges Gielen, KU Leuven, BE  
Geert Van der Plas, KU Leuven, BE

The growth of wireless services and other telecom applications increases the need for low-cost highly integrated solutions with very demanding performance specifications. This requires the development of intelligent front-end architectures that circumvent the physical limitations posed by the technology. In addition, with the evolution towards ultra deep submicron CMOS technologies, the design of SoC will emerge which are increasingly mixed-signal designs. The desire to do hand-crafted, one-transistor-at-a-time analogue design is increasingly at odds with the current time-to-market constraints and hence the need for more analogue design productivity, practical circuit and layout synthesis, and reliable verification at all levels of the mixed-signal hierarchy.

This tutorial will present the recent progress and current state-of-the-art in design tools and methodologies for complex mixed-signal designs as well as for RF IC design. Different aspects will be covered ranging from design methodologies and behavioural modelling to techniques for analogue circuit and layout synthesis. The techniques will be addressed from a designer point of view, so that attendees can assess how the techniques could be integrated to improve their current design practice.

The tutorial will also include on-line demonstrations of advanced research tools in this area so that attendees can get an even better idea of the capabilities and power of the presented material.

## **A2 Platform Based Design**

Organizer: Rolf Ernst, TU Braunschweig, DE  
Speakers: Rolf Ernst, TU Braunschweig, DE  
Michael Münch, Alcatel, BE

Platform based design uses architecture templates and libraries of complex configurable hardware and software components to reach the productivity required for complex System-on-Chips (SoC) design. Platform design methodologies must go hand-in-hand with architecture and library development to enable efficient mapping of applications to platforms. The tutorial will give insight to the architectures and methodologies of platform based SoC design and highlight some of the open issues and caveats.

In the introduction, we will define platform-based design from both an application as well as an architectural perspective. We will identify system components and investigate various design decisions that have to be made when designing platform architectures and components that can serve as generic building blocks in platform-based design. We will then discuss the necessary support in design methodology required to enable an efficient design

process around such platforms.

The second part of the tutorial will illustrate some of these issues through the design of a generic embedded processor-based platform designed and in use across various business divisions in Alcatel. Emphasis will be put on architectural trade-offs, as well as modelling and validation of designs based on the platform.

In the third part of the tutorial, we will highlight some of the tough design problems which arise from integration of heterogeneous hardware and software IP components on a platform. We will focus on performance and load analysis and optimisation in the context of multiprocessor platforms running real-time operating systems.

## **B2 Low Power Hardware Design**

Organizer: Wolfgang Nebel, OFFIS, DE  
Speakers: Wolfgang Nebel, OFFIS, DE  
Eike Schmidt, OFFIS, DE

This tutorial addresses system-level, algorithm, and RTL designers who are facing power problems in their designs. Power consumption is not a second-class citizen any more. More and more ASIC design projects have constraints on the power consumption. The constraints might be due to the chip package, reliability issues, or the battery lifetime of mobile applications.

This tutorial presents techniques to estimate and minimise power consumption of ASIC hardware implementations. Different levels of abstraction are addressed. The first part gives a brief overview of available power estimation tools and the underlying methodologies. Transistor, gate, RT, algorithm, and system-level tools and techniques are presented.

The second part discusses design techniques to minimise power and energy consumption. The tutorial focuses on the higher levels of abstraction, from system down to RT level, where most power savings can be gained. For system level optimisation, techniques like power management, bus encoding, data compression, memory hierarchy optimisation as well as voltage and frequency scaling are presented. Also addressed are approaches like algorithm selection, algorithm transformations, and common case computation. Examples of RT-level optimisation techniques which will be discussed are memory access optimisations, resource sharing and parallelisation, operand isolation, as well as clock gating.

## **C2 Design and Testing Challenges for Low-Voltage Scaled CMOS Circuits**

Organizer: Kaushik Roy, Purdue U, US  
Speakers: Kaushik Roy, Purdue U, US  
Ali Keshavarzi, Intel, US

This tutorial focuses on challenges of low-voltage CMOS design and test. As technology scales, leakage and leakage control becomes critical for design and test of integrated circuits. We explain test techniques for intrinsically leaky ICs and present measured data from industry. The following topics will be covered in detail: Scaling of MOS devices; Low voltage CMOS design styles; Cross-talk and predictable design; Transistor threshold scaling for high-performance designs; Leakage currents in CMOS circuits; Leakage control such as multiple  $V_t$  CMOS, dynamic  $V_t$  CMOS, transistor stacking and their implication to testing; Testing of low-voltage, low-threshold CMOS circuit and memories under elevated background leakage; Dynamic current testing; BIST for low-power circuits.

This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2002

## **E2 Test-Based Methods for Design Verification and Diagnosis**

Organizer: Dhiraj K. Pradhan, Bristol U, UK

Speaker: Dhiraj K. Pradhan, Bristol U, UK

Adit Singh, Auburn U, US

The interplay between test and design is becoming ever-more crucial. Often, manufacturing problems are, in fact, rooted in design problems. Consequently, understanding design verification helps test engineers in communicating with design engineers. Completion of this tutorial will help facilitate communication between test and design groups. This tutorial is aimed at giving test engineers an introduction to the use of test techniques for design verification and diagnosis. The following topics will be covered:

- Basic concepts of design flow
- Basic concepts of logic verification
- Application of test concepts and techniques to design verification
- Application of test concepts and techniques to design diagnosis

Both combinational and sequential circuit design verification and diagnosis will be discussed.

This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2002