An EMC-Compliant Design Method for High-density Integrated Circuits

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Abstract

This paper deals with an innovative method of EMC-compliant design. This technique helps to optimize emission level as soon as in the design phase, and provides noise-related solutions which will be evaluated and integrated into the silicon.

This method allows to model the activity of thousand-gate circuits thanks to only two current generators which represent supply current consumption in the VDD and the VSS rails.

This allows EMC evaluation and optimization (conducted noise) for a packaged integrated circuit within its electrical environment.

1.Introduction

When evaluating conducted emission in an integrated circuit, simulating digital blocks at the analog (transistors + parasitics) level is a time-consuming task, which is often performed by a Spice-like tool. Therefore, the circuit should not exceed approximately ten thousand gates. Consequently, it becomes important to find a new method allowing to reduce time and file size while preserving accuracy.

Core activity is modeled thanks to only two generators which represent supply current consumption in the VDD and the VSS rails. In addition to that, the generators can be associated to the system power supply, which can be measured or obtained from the PCB layout, or even described at device level.

2. An evaluation and optimization method for conducted emission

The process is achieved in four steps:

1. ivss/ivdd current modeling thanks to a logic simulator,
2. Environmental modeling (reference) (package, decoupling capacitor, PCB …),
3. Conducted emission evaluation thanks to an analog simulator like Spice,
4. Optimization according to a given specification.

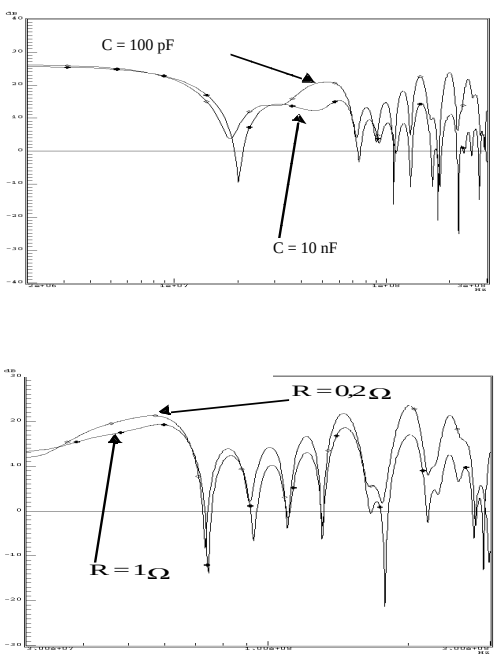
This environment can be described in two ways :

1. accurate description of the power supply network and of its interconnections,

2. measurement of the environment itself thanks to a network analyzer.

Evaluation can be done in the time domain or in the frequency domain.

Two examples are shown below. In the first example, the decoupling capacitor undergoes an optimization after which we can notice that noise level is better : 15 to 20 dB gain at 20 MHz and above. The second example shows the maximum resistance of the package, and how to reduce conducted noise level (10 dB).



Effects of decoupling capacitor and package resistance on noise level

3. Conclusion

This method helps the designer to control emission level in conducted mode with good accuracy. In particular, it enables to better quantify noise reduction right from the circuit environment. In addition to that, it allows the designer to test the architecture before the integrated circuit goes to the foundry.