A Fast Johnson-Mobius Encoding Scheme for Fault Secure Binary Counters[1]

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1. Introduction

The major characteristic of a counting unit is its performance. The basic properties that a fast counter must have are: i) high counting rate, preferably independent of the counter size, ii) a binary output; read on-the-fly, iii) sampling rate equal to the counting rate, and iv) a regular implementation suitable for VLSI.

For safety critical applications, the synchronous operation of a fault-secure binary counter makes reading the counter's value difficult and reduces the counting rate proportionally to counter's size. In this paper an implementation of a fault-secure binary counter using the Johnson-Mobius encoding scheme is presented.

2. Basic theory on Fault-Secure circuits

A circuit is called *Fault-Secure* with respect to a fault set **F**, if and only if, for every single fault and for all code word inputs the circuit will never produce an incorrect code word output. A hypothesis that when an error is present in a circuit, a second one may appear, after enough time for the first one to be detected, is made. This hypothesis may seem convenient but it is fully realistic. It is very hard that two errors appear simultaneously.

3. The 4-bit binary Johnson-Mobius module

The 5-bit modified Johnson-Mobius coded output of the circuit illustrated in Fig. 1, can give through proper modifications, a 4 bit simple binary output read on-the-fly. Binary counter units can be implemented using the modified 4-bit Johnson-Mobius counter unit. This 4-bit module was chosen to implement Johnson-Mobius counters with more counting states.

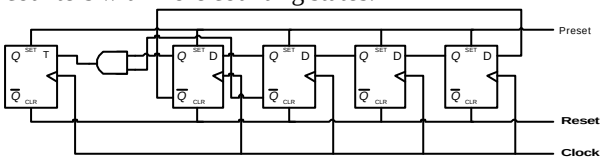

Fig. 1. Modified 4 bit Johnson-Mobius coded counter with 16 counting states

4. Johnson-Mobius Parity prediction scheme

Johnson-Mobius encoding scheme is considered as a Gray-like coding scheme. Thus the parity of the output of the 4-bit counter module can be predicted; every state transition flips the parity of the output. This observation, plus the fact that the parity of the modified Johnson-Mobius module changes in every state transition lead to the parity prediction scheme. The predicted parity is derived from a T-FF which is enabled to change state every clock cycle except for the one that the sequence $Q_3Q_2Q_1Q_0$ is "1000". Note that the initial value of the T flip/flop must correspond to the parity of the initial state of the JM counter.

In order to achieve high fault coverage the 4 bit counter module based on the Johnson-Mobius Code must be designed to be fault secure. That means that under any single fault that might happen during operation, the errors generated on the counter outputs (4 bit binary output) are single and thus are detected by the parity code.

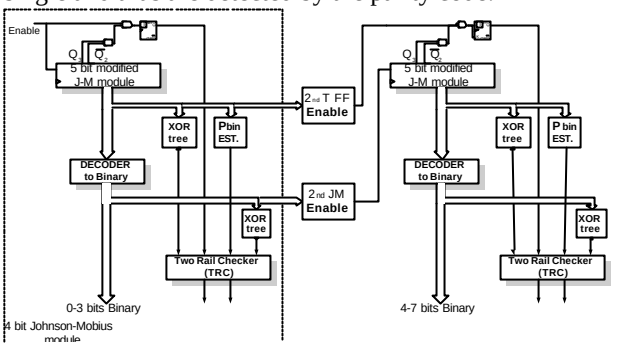

Fig. 2. 8-bit Johnson-Mobius FS binary counter architectural scheme

The 8-bit implementation scheme for the proposed counter is constructed from two identical 4-bit Johnson-Mobius encoded modules, with extra logic in between. The purpose of this logic is primary to enable the 2nd module only whenever it is needed. This enabling circuitry is the reason for the increased performance of the proposed counter. In simple words the next module's state transition does not depend on the concurrent transition of the preceding JM counter module, but only from its previous transition.

6. Experimental results

The synchronous binary counter and the conventional FS counter (doubling technique) were realized and compared to the presented counter. The normalized results in terms of performance are shown in table 1.

Table 1. Comparison of the three FS counters in terms of performance (delay time)

Counter type	4 bit	8 bit	16 bit	32 bit	64 bit
FS binary counter	1.65	1.69	1.67	1.62	1.52
Double binary counter	1.08	1.05	1.03	1.02	1.01
JM FS counter	1.71	1.16	0.86	0.69	0.59

7. Conclusions

The presented Johnson-Mobius counter architecture ensures the Fault-Secure property with the use of the parity prediction units. The extracted results showed that it presents much better performance, when compared to the other FS counter designs.

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