A Parallel LCC Simulation System

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Abstract

Cycle-based simulation at RT- and gate level realized by a Levelized Compiled Code (LCC) technique represents a well established method for functional verification in processor design. We present a parallel LCC simulation system developed to run on loosely-coupled processor systems allowing significant simulation acceleration. It comprises three parallel simulators and a complex model partitioning environment. A key idea of our approach is to valuate circuit model partitions with respect to the expected parallel simulation run-time and to integrate corresponding cost functions into partitioning algorithms. Experimental results are given with respect to IBM processor models of different size.

1. Parallelization Approach

TEXSIM and its successor MVLSIM are LCC simulators developed by IBM for the functional verification in microprocessor design. We have parallelized them for loosely-coupled processor systems (such as parallel IBM SP machines or IBM RS/6000 workstation clusters) following the *replicated worker principle*. This means replicating the sequential simulator and extending it by communication and synchronization facilities. During parallel simulation, n simulator instances cooperate, each instance handling a part of the original circuit model. Two of the resulting simulators, parallelTEXSIM [1] and parallelMVLSIM, are statically balanced. The simulator dlbSIM [3] is capable of dynamically balancing the application-specific load of simulator instances in dependence of the overall load situation on involved processor nodes. With dlbSIM, at any point of simulation run-time a simulator instance handles a subset of an initially assigned set of model parts.

2. Circuit Model Partitioning

Taking special *fan-in cones* as basic building blocks for partitions, we achieve a concentration of necessary synchronization and communication between simulator instances at cycle boundaries. Our complex partitioning environment parallelMAP allows combination and competition of algorithms within a hierarchical partitioning strategy. Partitioning is guided by a partition valuation function [2] comprising parameters related to both the circuit to be simulated and the host system the simulation is intended to run on. This way, run-time estimation of parallel simulation processes starting from circuit model partitions is possible.

3. Experimental Results

We consider five circuit models representing processor structures of the IBM S/390 architecture. The number of their boxes at RT/gate level is given in brackets: CLKSTR6 (187120), PICMOFP (235721), PU_M5X (252982), MBA98 (512843), ML100M0S (2657165). Figure 1 shows the expected speed-up of parallelMVLSIM simulation runs on an IBM SP2 machine in dependence of the number of processors (simulator instances).

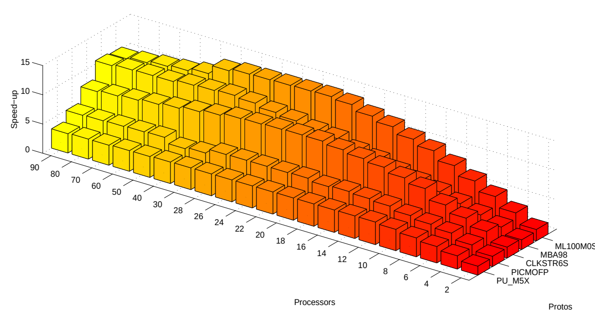

Figure 1. Expected simulation speed-up

References

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[2] K. Hering, R. Haupt, and U. Petri. Parameterized partition valuation for parallel logic simulation. In *Proc. of PDCN'97*, pages 144–150, 1997.

[3] K. Hering, J. Löser, and J. Markwardt. dlbSIM - a parallel functional logic simulator allowing dynamic load balancing. In *Proc. of DATE'01*, pages 472–478, 2001.