DAISY–CT: A High–Level Simulation Tool for Continuous–Time ΔΣ Modulators

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Abstract

To reduce the long circuit–level simulation time of ΔΣ modulators, a variety of techniques and tools exist that use high–level models for discrete–time (DT) ΔΣ modulators. There is, however, no rigorous methodology implemented in a tool for the continuous–time (CT) counterpart. Therefore, we have developed a methodology for the high–level simulation of CT ΔΣ modulators and implemented this method in a user–friendly tool. Key features are the simulation speed, accuracy and extensibility. Nonidealities such as finite gain, finite GBW, output impedance and also the important effect of jitter are modelled. Finally, experiments were carried out using the tool, exploring important design trade–offs.

Circuit–level simulation of ΔΣ modulators is too time consuming in most practical cases. Especially in the case where parameter analyses (sweeps) are needed or when a complete synthesis loop is wanted, an alternative needs to be found. In the approach presented, we therefore propose a behavioral modeling method. It is possible to view the modulator as a system implementing a set of mathematical equations. This leads to a behavioral model of the modulator and its nonidealities. For a first order system this gives:

$$x(kT) = x((k-1)T) + \frac{1}{T}\int_{(k-1)T}^{kT} u(\tau)\,d\tau - \frac{1}{T}\int_{(k-1)T}^{kT} y(\tau)\,d\tau \quad (1)$$

The simulation speed of this approach is comparable with the simulation of DT modulators. Of course, there is some speed penalty due to the calculations of the integrals, but this can be kept minimal if they are calculated analytically instead of numerically. With this approach a sampled version of both output and internal state variables is obtained.

Several nonidealities, such as finite gain, finite GBW, output impedance, jitter, etc., are covered in the proposed tool. The user can, however, also map his own models by deriving the values for the generic coefficients.

Table 1 shows the inputs of a design exploration experiment that resulted in the plot of figure 1. From this picture it can be concluded that, in order not to degrade the performance, the opamp ouput impedance should be between 3 to 10 kΩ (the top 2 lines) and the allowable pulse width jitter is 0.01 % of the clock period.

Table 1. Inputs for the example.

Parameter	Value
topology	CT single–loop, third order
OSR / f_s	48 / 50 MHz
input amplitude, / f_i	0.25 V / 100 kHz
reference voltage	1 V
integrator type	OPAMP–C
DAC type	return–to–zero (PW = 80 %)
finite opamp gain / GBW	60 dB / 100 Mhz
finite opamp R_{out}	1K / 3K / 10K
opamp input capacitance	1 pF
pulse width jitter	1E-5 . . . 1E-2

We conclude that the proposed methodology is promising for the high–level simulation of CT ΔΣ modulators and that the developed tool allows to efficiently find design trade–offs.

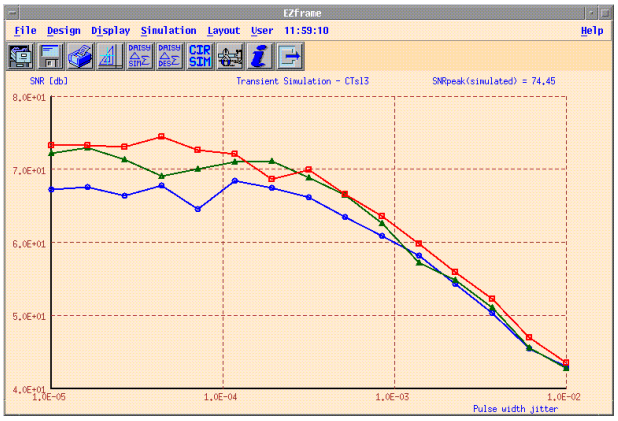

Figure 1. The effect of pulse width jitter on SNR for different output impedances.