

A SAT Solver Using Software and Reconfigurable Hardware*

Iouliia Skliarova, António B. Ferrari

iouliia@ua.pt, ferrari@ieeta.pt

Department of Electronics and Telecommunications

University of Aveiro

3810-193 Aveiro, Portugal

Abstract

In this paper we propose a novel approach for solving the Boolean satisfiability problem by combining software and reconfigurable hardware. The suggested technique avoids instance-specific hardware compilation and, as a result, achieves a higher performance than pure software approaches. Moreover, it permits problems that exceed the resources of the available reconfigurable hardware to be solved.

The Boolean satisfiability problem (SAT) consists in determining if a formula in CNF (Conjunctive Normal Form) is satisfiable, i.e. whether there exists an assignment of values to variables that forces the formula to evaluate to 1. It should be noted that SAT is an NP-complete problem. Thus the complexity of the respective algorithms makes it difficult (and sometimes even impossible) to solve the problem in a reasonable time, or with the available computational resources. As a result, new techniques for accelerating the solution of SAT are constantly being proposed, either in software or in hardware.

The majority of researches in the area of accelerating SAT solutions with the aid of reconfigurable hardware apply an instance-specific approach, i.e. they generate a specialized hardware circuit for each Boolean formula to be considered. However, this method can only be used effectively for tasks with a large volume of input data where the hardware compilation time is offset by the reduced execution time.

We formulate the SAT problem over a ternary matrix \mathbf{M} by setting a correspondence between clauses and rows of \mathbf{M} , and between variables and columns of \mathbf{M} . Note that the problem of satisfying the Boolean formula is equivalent to finding a ternary vector \mathbf{v} , which is orthogonal to each row of the corresponding matrix \mathbf{M} . In order to solve the SAT problem formulated in terms of a ternary matrix we apply a backtracking search algorithm, which is similar to the well-known Davis-Putnam procedure. The proposed satisfier architecture is depicted in fig. 1.

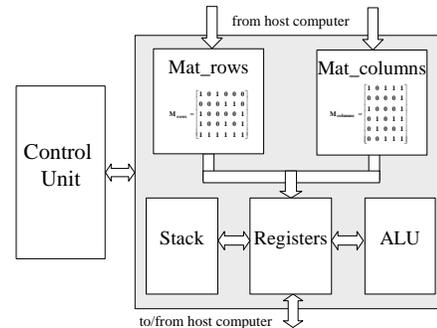


Figure 1. The proposed satisfier architecture.

In order to solve various problem instances it is only necessary to download the respective matrix data. All the other components of the satisfier remain unchanged. It allows utilizing local reconfigurability and reduces configuration overhead.

The satisfier was implemented on an ADM-XRC PCI board containing one XCV812E Virtex Extended Memory FPGA, which is very well suited to the proposed architecture of a SAT solver because we can use a large amount of RAM blocks to store matrices.

Another important issue affecting any algorithm implemented on reconfigurable hardware is related to the capacity of the hardware platform. Because of that we developed a special strategy that allows to partition the problem between software and reconfigurable hardware. In this case, an FPGA will only be responsible for processing sub-problems that appear at various levels of the decision tree and satisfy the imposed hardware constraints (such as the maximum allowed number of rows and columns in the matrix). This technique permits problems to be solved that exceed the resources of the available reconfigurable hardware.

The results of experiments on some of DIMACS benchmarks have shown that using our approach it is possible to achieve a significant speedup compared to the state-of-the-art software SAT solver GRASP (up to 111x, including the FPGA configuration time, being GRASP executed on an AMD Athlon/1GHz/256MB).

* This work was sponsored by the grant FCT-PRAXIS XXI/BD/21353/99