A Complete Phase-Locked Loop Power Consumption Model*

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Abstract

A PLL power model that accurately estimates the power consumption during both lock and acquisition states is presented. The model is within 5% of circuit level simulation (SPICE) values. No significant power overhead (+/- 5% of the power consumed at the final frequency) is incurred during the acquisition process.

1. The PLL dynamic behavior

The PLL can be described as a 2nd order continuous time system. For a step of magnitude A_{step} in the input frequency, the time response is given by:

$$f_o(t) = A_{step} N \left[1 - (1/\omega_d) e^{-\xi\omega_n t} \cos\left(\omega_n \sqrt{1-\xi^2}\, t + \sin^{-1}(\xi\omega_n)\right)\right]$$

$$\xi = \frac{R}{2}\sqrt{\left(\frac{1}{N}\right) K_V I_{CH} C} \quad ; \quad \omega_n = \sqrt{\frac{K_V I_{CH}}{CN}}$$

If the frequency step takes the VCO frequency beyond the lock range, then a capture (pull-in) process takes place initially. Otherwise, only a lock process occurs, which is defined by t_{lock}. These times can be expressed as:

$$t_{lock} \approx \frac{1}{\xi\omega_n} \quad ; \quad t_{capture} = \left| f_o(t_{capture}) - f_o(0) \right| \frac{2C}{K_V I_{CH}}$$

For the VCO gain K_V (Hz/V), we need to calculate:

$$K_V = \frac{df}{dV_C} = \frac{k(V_{ds}) w C_{ox} v_{sat}}{2nV_{sw} C_{cell}}$$

Various differential and single-ended VCOs with different values of *n* were implemented using Berkeley's MAGIC CAD tool in a 0.35um technology, operating with a 2.5V supply voltage. This is the validation framework for all other experiments. The average error for the estimated K_V data was 2.2% and 3.2% for non-differential and differential implementations, respectively.

The resistor (*R*) was built as a transmission gate with both devices always on. Since V_{DS} is small and assuming that V_{GS} is on average close to $V_{dd}/2$, thus:

$$R_T = \frac{V_{DS}}{I_D} = \frac{2}{k(V_{DS}) \mu_n C_{ox} (V_{dd} - 2V_T)} \left(\frac{L}{W}\right)$$

The average deviation with respect to the simulated values was 3.77% and 3.2%, for *n* and *p* devices respectively. The charge pump current (I_{CH}) and the filter capacitance (*C*) are described by equations already available.

2. PLL power model

For an *n*-stage differential and non-differential VCO design, the effective capacitances are:

$$C_{vco-diff} = 2n^2 k C_{cell} = 2n^2 k \left[W_n (C_{gate} + C_{drain\_n}) + 2W_p C_{drain\_p}\right]$$

$$C_{vco-nodiff} = 2nC_{cell} = \left[W_n (C_{gate} + C_{drain\_n}) + W_p (C_{gate} + C_{drain\_p})\right]$$

Where *k* defines the voltage swing of each cell ($V_{sw}=kV_{dd}$) and W_p and W_n, the normalized width of the *n* and *p* devices. For the PFD:

$$C_{eff-pfd} = N_{tpfd} G_{pfd} C_{tech}$$

Where, N_{tpfd} = 146, $G_{pfd-lock}$ =0.74 (during acquisition, $G_{pfd-acq}$ = 0.83) and $C_{tech} = C_{gate} + C_{drain\_ave}$. A similar equation can be applied to the FDIV, using N_{tfdiv} = 104 and G_{fdiv} = 0.78.

For the charge pump, the total energy delivered is expressed as a function of the total variation of the capacitor voltage *(ΔV)* during the capture process. Thus:

$$P_{CH-PUMP} = \left(\frac{\Delta V^2 C}{t_{capture}}\right) + \left(\frac{\Delta V \cdot C}{t_{capture}}\right)^2 R = \left(\frac{\Delta V \cdot I_{CH}}{2}\right) + \left(\frac{I_{CH}^2 \cdot R}{4}\right)$$

We calculate the contribution of the bias circuitry as proportional to I_{CH}. During lock, the total PLL power is:

$$P_{PLL\_lock} = \left[N_{tpfd} G_{pfd} + N\left(2n(6) + N_{tfdiv} G_{fdiv}\right)\right] C_{tech} V_{dd}^2 f_{ext} + I_{bias} V_{dd}$$

The average error from the simulated results was 3.5% and 3.4% across all non-differential and differential designs. The power consumption during acquisition:

$$P_{PLL\_acq} = \frac{1}{t_{acq}} \left(P_{PLL\_lock-in} t_{lock} + P_{PLL\_capture} t_{capture}\right)$$

The PLL power consumption during capture is (for the PFD, $G_{pfd-acq}$ is used):

$$P_{PLL\_capture} = \left(C_{PFD} + C_{VCO} + C_{FDIV}\right) V_{dd}^2 f_{capture\_ave} + P_{bias} + P_{ch\_pump}$$

Where $f_{capture\_ave}$ is the mean value between the start and stop frequencies during the capture process. For the lock process, a similar equation is used but a different $f_{capture\_lock}$ is estimated using the definition of average value. This calculated average was within 1% of the final target frequency. The average deviation from the SPICE readings was 1.7% and 0.7% for all non-differential and differential designs.

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