The Selective Pull-up (SP) Noise Immunity Scheme for Dynamic Circuits

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Noise is an important consideration in the design of integrated circuits. Increased immunity to noise, however, typically comes at the expense of increased delay. So, it is very important to have an adequate noise immunity with a minimum penalty in performance. "Global" noise immunity schemes can be used when the noise is approximately the same on all nodes in the circuit; but when a few nodes are noisier then others much better results can be obtained by selective noise immunity schemes.

The Selective Pull-up (SP) technique for dynamic circuits is a method for improving the noise immunity of inputs *selectively*, so that the least penalty in delay is paid for inputs that intrinsically have higher noise immunity.

The previously proposed *Inverter* selective immunity scheme applied to a NAND gate is shown in Fig. 1(a). The technique consists of adding a pull-up PMOS transistor for each NMOS transistor in the pull-down network in a virtual *inverter-like* configuration, but works only for networks without branches.

The Selective Pull-up (SP) technique is a generalization of the Inverter scheme that can be applied to arbitrary networks as follows:

- identify all the electrical nodes in the pull-down network, including the output node,

- identify all the NMOS transistor drains that are connected to each node (excluding any *precharge* transistors),

- create a pull-up network formed of a stack of series PMOS transistors for each node that has (NMOS) drains connected to it. The gate of each PMOS transistor is connected to the gate of the corresponding NMOS transistor.

- size the PMOS transistors in order to achieve the required noise immunity. A PMOS transistor with a greater width will provide more noise immunity, but lower performance, and *vice-versa*.

The SP technique applied to an AOI gate and an OR gate is shown in Fig. 1(b) and 1(c). For a circuit with no branches in the pull-down (e.g. NAND gate), the circuit reduces to the same as for the Inverter technique, as in Fig. 1(a). For a circuit with no other nodes in the pull-down except the output node (e.g. OR gate), the SP technique reduces to the equivalent static gate plus the precharge and evaluate transistors, as in Fig. 1(c).

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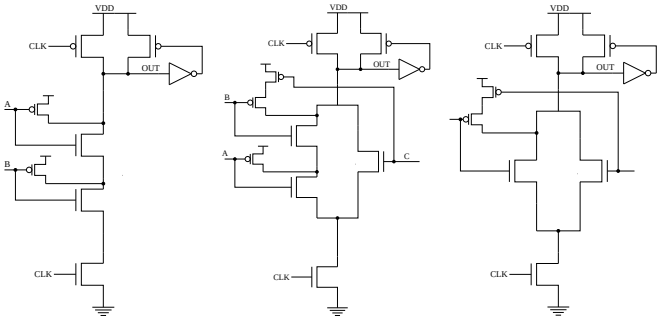

Figure 1. (a) The Inverter technique, the SP technique applied to (b) AOI gate, (c) OR gate.

keeper (*nm*)	SP - A (*nm*)	SP - B (*nm*)	SP - C (*nm*)	delay (*ps*)	current (μA)
400	400	400	400	56.77	179
400	600	600	600	57.37	188.1
No SP					
400	-	-	-	52.59	148.9
1017	-	-	-	61.07	161.1

Table 1. Comparison of delay and currents

Noise immunity curves were used for comparing different noise immunity schemes, with amplitude of the noise pulse on the X axis, and the width of the noise pulse on the Y axis. Extensive simulations show the increased performance achievable with the SP technique compared to other schemes, for a given noise immunity. Table 1 shows the comparison of the delay and average currents for the AOI with different keeper sizes with or wihtout the SP technique. In order to obtain the same noise immunity as for the SP technique a much larger keeper size is needed which significantly affects performance (last row in the table).

The SP technique performs better than other noise immunity schemes especially when the noise is different on different nodes of the circuit. Identifying noisier nodes in a circuit is still a challenge for current CAD tools.