High-Level Modeling and Design of Asynchronous Arbiters for On-Chip Communication Systems

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Abstract *This poster presents the design of complex arbitration modules, like those required in SoC communication systems. Clock-less, delay-insensitive arbiters are studied in the perspective of making easier and more practical the design of future GALS or GALA SoCs. This work focuses on high-level modeling and delay-insensitive implementations of low-power and reliable fixed and dynamic priority arbiters.*

Design flow The design flow used to synthesize asynchronous circuits (figure 1) starts from a high-level modeling using CHP (Communicating Hardware Processes). The CHP language [2] is naturally adopted because i) it includes non deterministic choice structures required to model arbitration, and ii) it is very well suited to model and synthesize delay-insensitive circuits [2][3].

TAST extracts from the CHP programs VHDL gate-level netlists that are verified by back-annotable logic simulations with timing [4]. A standard-cell library and a specific asynchronous-cell library are targeted. Circuit netlists are imported into backend tools for electrical simulations, placement and routing. The technology used is the 0.18 µm CMOS process from STMicroelectronics.

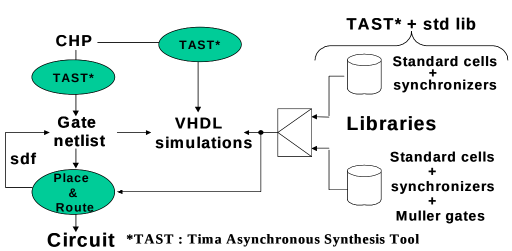

Figure 1. Design flow overview

Fixed/dynamic priority arbiters Fixed-priority arbiters have to choose among input requests with predefined hardware-coded priority values. In a dynamic-priority arbiter, each input channel carries requests with priority values. The dynamic-priority arbiter performs comparisons and grants the active requests with the highest priority value. The poster compares several traditional arbitration algorithms with a two-stage priority-arbiter [1]. This parallel-request-sampler arbiter decouples request signals sampling and contention solving. The first stage of synchronizer blocks samples all the request signals as soon as at least one of them is becoming active. It then passes the request-signal samples to the second stage which is in charge of selecting the request to serve first. This stage can implement fixed or dynamic-priority resolution algorithm.

Results Pre-layout electrical simulations report that delay-insensitive arbiters processing hundreds million requests per second can be designed using an up-to-date CMOS technology. These structures outperform previously proposed structures in terms of complexity and latency.

The proposed arbiters are modular, scalable, hundred percent reliable (enough time is given to resolve metastability), and of low-complexity ("n" synchronizers for "n" input-requests plus a combinational block which complexity is $\log_2(n)$). Finally, these asynchronous priority arbiters are low-power: they do not consume in absence of request (event-driven instead of clocked).

Conclusion This work is the first step toward the synthesis of complex arbitration schemes from high-level behavioral specifications. Prospective works will be focused on the complete automation of the synthesis process and the improvement of arbiter architecture and circuit performances. "n to p" fixed or dynamic priority routers will also be investigated to address the design of complex on-chip routing systems.

The full paper is available at **http://tima.imag.fr/cis/**

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