An Encoding Technique for Low Power CMOS Implementations of Controllers

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Abstract

Power consumption is becoming one of the most critical parameters in VLSI design. In this paper we describe a novel state assignment algorithm targeting towards low power CMOS realizations of controllers. The main features of the new approach can be summarized as follows: 1) flexible column encoding strategy which allows handling the area and the register activity cost functions separately and 2) preliminary analysis of the FSM to control relative weight of each cost function. Experimental results show that on average there is a 25% reduction in power consumption compared to an standard tool and without area penalty.

1 Introduction

It is well known that the main contributor to power consumption in CMOS circuits is dynamic power dissipation which depends on the switching activity of the circuit. Through state assignment the switching activity of some gates in the circuit can be reduced. In particular, the switching activity of the memory elements depends on the state encoding chosen for the states. Since the state assignment also influences the complexity (number of gates and capacitances) of the combinational component, it is well accepted that low power state assignment algorithms must take into account power consumption in the combinational component, and so area must be included as a target in addition to the register switching activity. Thus, most contributions approach the state assignment for low power as a multi-criteria problem [1-5]. However, they have limitations concerning balancing of both criteria, register activity and area, because optimal choice of relative weights strongly depends on the machine structure. The algorithm we propose automatically adapts the relative effort dedicated to each target on the basis of a collection of parameters which can be obtained from the initial FSM description.

2 The New Algorithm

In order to overcome limitations of previously reported algorithms, we resort to a column based state assignment approach. That is, the encoding is built column by column. This allows working separately with both targets by devoting a number, m_A, of columns to the satisfaction of face constraints and the remaining columns to register switching activity reduction. In the area oriented step the optimization criterion is the economical implementation of face constraints [6]. The second step targets minimization of the register switching activity by assigning codes with a low Hamming distance to pairs of states with a high transition probability [2].

The advantage of this strategy is that the conflict arising from the clearly distinct nature of both objectives is avoided. In addition, m_A determines the relative weight of both targets. An efficient heuristic for deriving m_A from the symbolic description of each machine has been incorporated into the algorithm. It takes into account the following parameters: 1) the probability that at least one register is active per clock cycle. It is obtained by a probabilistic analysis of the FSM modeled as a discrete Markov-chain [2]; 2) number of encoding bits; 3) ratio between the number of face constraints and the cardinality of the minimal symbolic description of the FSM.

3 Results

Table below compares relatively to JEDI different algorithms for low power state assignment: *LPSA* [1], *POW3* [2], [3], and the proposed algorithm called *PICOLA_POWER*.

	POW3	*from [3]*	*LPSA*	*PICOLA_POWER*
Power	-16%	- 21%	-16%	- 25%
Area	7%	-3%	4%	- 4%

4References

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