I_{DDT} Testing of Embedded CMOS SRAMs

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Summary

This paper presents an i_{DDT} test method for embedded CMOS SRAMs. A total of 192 faults were inserted and simulated using parameters from a 0.35 um process. The SRAM model includes realistic effects such as wire bonding inductance and resistance parameters as well as bypass capacitance. A sensor is introduced and incorporated into the SRAM cell array to detect abnormal i_{DDT} switching. Figure 1 shows a 1-bit SRAM organized into 64 128 x 128 cell blocks with an i_{DDT} sensor monitoring each cell block. The SRAM model includes the following parameters:

??On-chip wire bonding inductance of 2 nH
??On-chip wire bond resistance of .01 Ohms
??On-chip bypass capacitance of 1 pF
??Bitline capacitance of 3 pF
??Power line capacitance of 40 pF

The results of the fault simulations comparing voltage, I_{DDQ} and i_{DDT} test methods are given in Table 1.

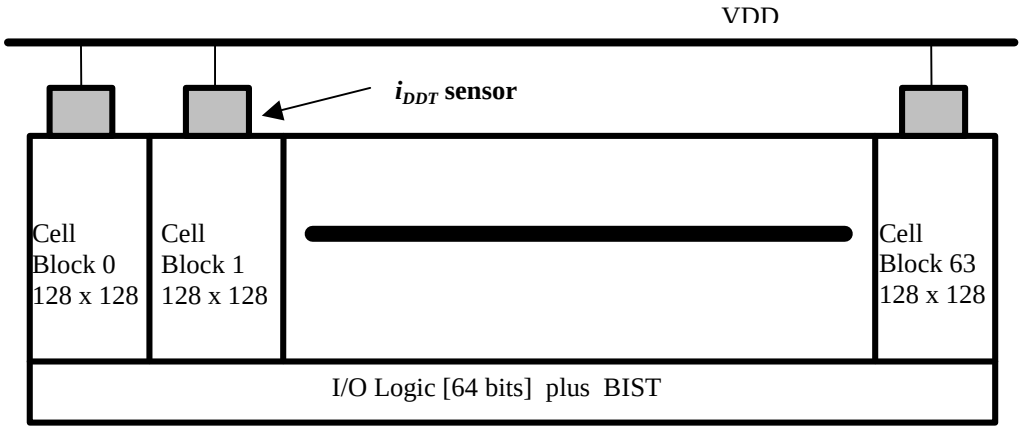

Figure 1. SRAM Model with Embedded i_{DDT} Sensors.

Faults	Voltage		I_{DDQ}		i_{DDT}	
	Detected	Undetected	Detected	Undetected	Detected	Undetected
Opens	31	32	4	59	63	0
Gate oxide shorts	17	1	12	6	18	0
Cell Bridging faults	44	16	40	20	60	0
Decoder faults	37	10	14	33	43	4
Pattern Sensitivity Faults	3	1	1	3	4	0
Total	132 (68.75%)	60 (31.25%)	71 (36.98%)	121 (63.02%)	188 (97.9%)	4

Table 1. Fault Simulation Results.