A New Formulation for SOC Floorplan Area Minimization Problem

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Abstract

In this poster, we presented a new formulation by introducing the concept of block partition such that the shape of modules can be automatically determined based on the goal of optimization. Experimental results from MCNC benchmarks indicate that the zero dead space solutions can be obtained for most test cases under our formulation.

1 Introduction

As VLSI designs entering the SOC era, IP blocks may come from different design methodologies in the floorplan stage and the shape of modules may not be predetermined.

Some proper formulations are required to minimize the chip area. Therefore, we introduce the concept of block partition and model it as a nonlinear programming problem. Fig. 1 shows that both of the total chip area and the inter-module wire length of critical nets are reduced after introducing the concept of block partition to describe soft modules with rectilinear shape.
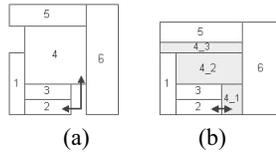

(a)   (b)

Fig.1 Reduce area and wire length by block partitioning.

2 Problem Formulation

Suppose that there are n modules and n_1 of these are hard type. A *basic block i* can be described by the corresponding constraints:

$x_i + w_i = \hat{x}_i$, $y_i + h_i = \hat{y}_i$, $A_i = h_i \times w_i$ and $r_i = h_i / w_i$

where (x_i, y_i) and $(\hat{x}_i, \hat{y}_i)$ are the coordinates of the bottom-left and top-right corners. when block i is a hard module, h_i, w_i and r_i are fixed. For a soft module j, we give an additional aspect ratio constraint $r_{j\_L} \leq r_j \leq r_{j\_H}$.

Assume module i is partitioned vertically into k_i basic blocks. The corresponding constraints are

$x_{i\_j} + w_{i\_j} = \hat{x}_{i\_j}$, $y_{i\_j} + h_{i\_j} = \hat{y}_{i\_j}$, $A_{i\_j} = h_{i\_j} \times w_{i\_j}$,

$A_i = \sum_{j=1}^{k_i} A_{i\_j}$, $\hat{x}_{i\_(p-1)} = x_{i\_p}$ where $j = 1, 2, ..., k_i$ and $p = 2, .., k_i$.

Constraints $\max\{ \hat{y}_{i\_p} - y_{i\_(p-1)}, \hat{y}_{i\_(p-1)} - y_{i\_p} \} < h_1 + h_2$

are added to guarantee the abutment relations of basic

blocks. Horizontally partition can be formulated similarly. Besides, we define the *height, width* and *aspect ratio* for *the partitioned soft module i* as:

$h_i = \max\{\hat{y}_{i\_1}, \hat{y}_{i\_2}, ..., \hat{y}_{i\_k_i}\} - \min\{y_{i\_1}, y_{i\_2}, ..., y_{i\_k_i}\}$,

$w_i = \max\{\hat{x}_{i\_1}, \hat{x}_{i\_2}, ..., \hat{x}_{i\_k_i}\} - \min\{x_{i\_1}, x_{i\_2}, ..., x_{i\_k_i}\}$, and

$r_i = h_i / w_i$. The aspect ratio constraint of a partitioned soft module i is defined as $r_{i\_L} \leq r_i \leq r_{i\_H}$. We can also define aspect ratio constraints on each basic sub-block. We developed an $O(n^2)$ algorithm to decide what modules will be partitioned. The area minimization problem is then formulated as:

Minimize $\mathbf{X \cdot Y}$
Subject to
Module constraints;
Topological constraints;

$\mathbf{X} = \mathbf{max} \{\hat{x}_i, \hat{x}_{m\_k_m} \mid 1 \leq i \leq n_1, n_1 + 1 \leq m \leq n\}$;

$\mathbf{Y} = \mathbf{max} \{\hat{y}_i, \hat{y}_{m\_k_m} \mid 1 \leq i \leq n_1, n_1 + 1 \leq m \leq n\}$;

3 Experimental Results and Conclusion

For four of five MCNC benchmarks we get the zero dead space optimal solution. Fig. 3 shows the zero deadspace placements of ami33. For ami49, we can further improved deadspace from 0.38% [1] to 0.28% by partitioning two modules. Our area minimization method with block partitioning can be applied as a post-process to further reduce the area and improve the interconnections between modules for outputs of all existing floorplanning algorithms.
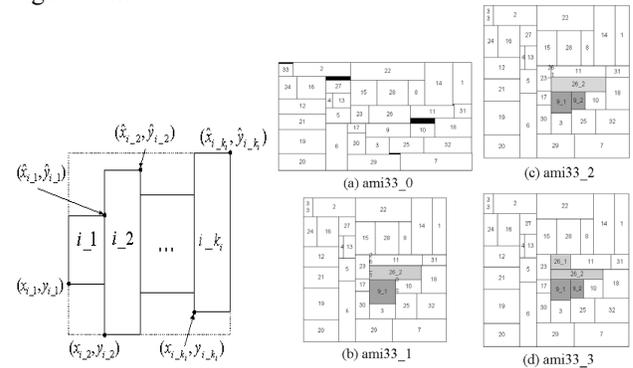

(a) ami33_0

(c) ami33_2

(b) ami33_1

(d) ami33_3

$(\hat{x}_{i\_2}, \hat{y}_{i\_2})$ $(\hat{x}_{i\_k_i}, \hat{y}_{i\_k_i})$

$(\hat{x}_{i\_1}, \hat{y}_{i\_1})$

i_1 i_2 ... i_k_i

(x_{i_1}, y_{i_1})

(x_{i_2}, y_{i_2}) $(x_{i\_k_i}, y_{i\_k_i})$

Fig. 2 Vertically partitioning **Fig. 3** Placements of ami33

Reference

[1] H. Murata and Ernest S. Kuh , "Sequence-Pair Based Placement Method for Hard/Soft/Pre-placed Modules", *International Symposium on Physical Design*, pp.167-172, Apr. 1998.