Self-Checking Scheme for the On-Line Testing of Power Supply Noise*

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Abstract

We propose a self-checking scheme for the on-line testing of power supply noise exceeding a tolerance bound to be chosen accordingly to system's constraints. Upon the occurrence of such a noise, our scheme provides an output error message, which can be exploited for diagnosis purposes or to recover from the detected noise (thus guaranteeing the system's correct operation). As far as we are concerned, no on-line testing scheme for power supply noise has been proposed up to now. Our scheme negligibly impacts system's performance, features self-checking ability with respect to a wide set of possible internal faults and keeps on revealing on-line the occurrence of power supply noise, despite the possible presence of noise affecting also ground.

1. Introduction

Power supply is generally distributed throughout a chip using a hierarchy of distribution networks. The occurrence of variations of the power supply voltage, hereafter referred to as power supply noise (PSN), has always been a major concern for any digital system and it is expected to increase significantly with the complexity and integration density of next generation, very deep sub-micron ICs.

Within a chip, PSN generally originates because of an excessive internal gates' activity. In fact, in the case of synchronous systems, the current pulses from the logic and memory blocks cause voltage drops across the resistive on-chip power distribution network. In particular, this is most likely to occur at the beginning/end of the clock periods, when the number of simultaneously switching latches/flip-flops is maximized [1].

Traditionally, bypass capacitors are used in order to filter out PSN. However, unless the loads draw a constant DC current, even the most carefully designed power distribution network presents some amount of supply noise. Since such a noise can not be avoided despite the use of bypass capacitors, there is generally also the attempt to reduce the effect of such a noise on system's operation through proper isolation of some sensitive circuits (e.g., delay lines) from power supply. As a result, PSN is generally managed through a proper combination of reduction and isolation [2].

Despite the adoption of these techniques, however, PSN still constitutes a major problem for high speed systems. As an example, in [3] Zhao et Al. report a PSN of $35\% V_{DD}$ for systems implemented using a 0.25 μm CMOS technology with V_{DD} = 2.5V, which obviously constitutes a noise too high to be possibly tolerated.

In addition, this problem is expected to worsen significantly for next generation very deep sub-micron ICs [4, 2]. In fact, with the increasing of ICs' density and complexity, there will be an increase in the number of simultaneously switching ICs, with consequent increase of probability of power supply variations' occurrence. Meanwhile, the increase in ICs' operating frequency will increase their sensitivity to the degradation of dynamic performance due to PSN, with possible consequent system's incorrect operation. Finally, also signal integrity may be significantly affected (for instance in the case of dynamic ICs) and this aspect will worsen with the reduction of circuits' noise margins with the scaling down of technology.

In this context, we propose a self-checking scheme for the on-line detection of PSN exceeding a tolerance bound (to be chosen accordingly to the considered system tolerance bound). Upon the occurrence of such a noise, our scheme provides an output error message, which can then be exploited for diagnosis purposes (e.g., if our detector is applied to test chips) or to recover from the detected noise (thus guaranteeing the system's correct operation).

As far as we are concerned, no on-line testing scheme for PSN has been proposed up to now.

The major difficulties in the on-line detection of such a noise are due to the fact that any scheme conceived to fulfill this purpose is in turn itself affected by the power supply noise to be detected. Reversely, the scheme proposed here is itself immune from such a sort of equalization phenomenon.

Our detecting scheme will be described as operating with

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a two-rail encoded synchronous system (as it is frequently the case for self-checking [5] synchronous systems). However, it could be used for general synchronous systems with unencoded outputs, by simply modifying its input stage.

Our scheme negligibly impacts system's performance, features self-checking ability with respect to a wide set of possible internal faults (including node stuck-ats, transistor stuck-ons, transistor stuck-opens, resistive bridgings, delays and transient faults) and keeps on revealing on-line the occurrence of PSN due to the simultaneous switching of an excessive number of gates, despite the possible presence of noise affecting also the ground signal.

Our detector is suitable to be implemented using custom and semi-custom VLSI, very deep submicron technology, as well as low cost Field Programmable Gate Arrays, by means of straightforward modifications.

This paper is organized as follows. In section 2, we introduce the basic idea behind our proposed scheme. In section 3, we describe its internal structure. In section 4, we show its possible VLSI implementation and report the results of the performed electrical level simulations. In section 5, we analyze its self-checking ability, while we draw some conclusive remarks in section 6.

2. Basic Idea

One possible idea to detect on-line the occurrence of PSN is to (indirectly) reveal it as a "delay fault" affecting a general IC of a considered system.

Unfortunately, we have verified that when a delay is due to PSN, it may not be detected by the existing on-line detectors for delay faults like, for instance, those in [6, 7, 8]. In fact, these detectors are themselves affected by PSN, which slows down their operation and, because of a sort of equalization phenomenon which takes place, they are in practice unable to reveal the delay due to PSN (differently from otherwise originated delay faults).

Based on these considerations, we propose a novel scheme which always tries to reveal the PSN indirectly (by detecting on-line the caused delay) but which, in order to avoid the equalization phenomenon discussed above, is based on the use of two sub-circuits whose noise-induced delay is, by design and due to the noise and detector's activating conditions themselves, different from one another.

As a result, upon the occurrence of PSN, our detector produces an output error message, while it gives an indication of correct operation in the absence of PSN.

Our detecting scheme is here introduced as operating with a two-rail encoded synchronous system (as it is frequently the case for self-checking [5] synchronous systems). However, as shown in the next section, it can be also used for synchronous systems with unencoded outputs.

3. The Proposed Power Supply Noise Detector

We consider the case of a generic synchronous system with busses encoded using the two-rail code, schematically represented in Fig. 1, where COMB denotes a generic combinational block with two-rail encoded outputs, FF_i and FF'_i (i = 1, ..., N) are system's flip-flops/latches sampling the COMB outputs, while $BUFF_i$ and $BUFF'_i$ are generic buffers driving such signals on a system bus.

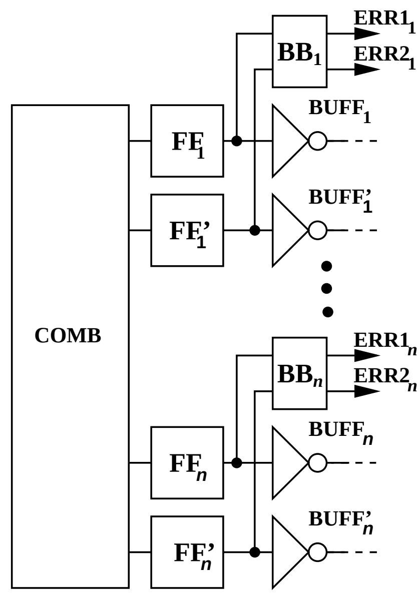

Figure 1. Schematic representation of the considered synchronous system.

Our proposed scheme consists of N Basic Blocks (BB_i, in Fig. 1), each receiving as inputs the two-railed outputs of a couple of FFs and giving the output signals ($ERR1_i, ERR2_i$).

In the absence of PSN, ($ERR1_i, ERR2_i$) = (01) or (10), $\forall i(i = 1, ..., N)$. Instead, if because of the simultaneous switching of an excessive number of FFs PSN arises [2], ($ERR1_i, ERR2_i$) = (00) or (11) for the switching FFs.

The outputs of the N basic blocks can then be joined together to obtain a global error/non-error indication by means of a simple two-rail code checker, for instance of the kind in [9, 10, 11, 12, 13, 14].

Let us now introduce the internal structure of our basic block. As shown in Fig. 2, it consists of an *input* and *output stage* directly connected to each other.

The *input* stage consists of two standard 2-input NAND gates (designed to be symmetric in the absence of PSN). An input of these two gates is connected to the power supply (V_{DD}), while the other is connected to the corresponding FF and FF' output, hereafter referred to as D_i and D'_i, respectively.

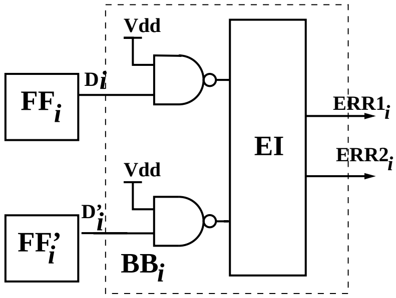

Figure 2. Schematic representation of the internal structure of our scheme basic block.

When D_i and D_i' have a transition, the outputs of these two gates change. Because of their symmetry, they feature equal low-to-high and high-to-low transition times. As a result, a (01) or (10) is produced at the two gates' outputs.

Instead, if PSN occurs (because of an excessive number of simultaneously switching FFs), a (00) or (11) appears at the NANDs' outputs, whose duration is proportional to the entity of PSN.

As an example, considering the case of 2 symmetric NANDs implemented by means of a 0.35μm CMOS technology with 3.3V power supply (V_{DD}), we have found an increase in the duration of the (00) or (11) indication with the increase of PSN of the kind shown in Fig. 3.

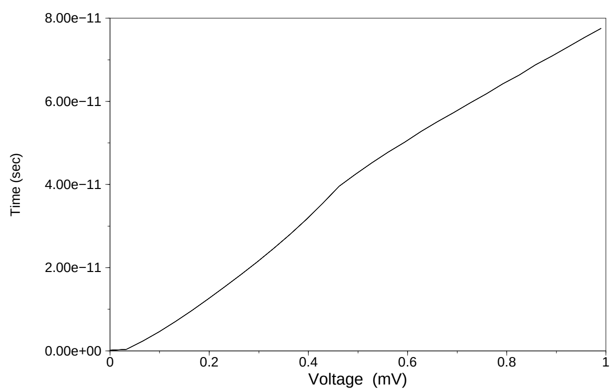

Figure 3. Duration of the error indication at the two NAND outputs as a function of the entity of PSN.

Therefore, by simply connecting to the output of the *input stage* an *output stage* (EI in Fig. 2) able to discriminate and latch upon the occurrence of a (00) or (11) with a duration corresponding to a PSN above the considered tolerable value, a detector for PSN can be obtained.

This can be achieved by using an *output stage* behaving like an "error indicator" [15, 16, 17] of the kind used at the outputs of checkers of self-checking circuits to discriminate and latch the produced output error indications with respect to the "spurious" ones, due to signals' transitions. Of course, as usual in the case of self-checking circuits, the considered error indicator should be designed to account also for variations of its sensitivity due to statistical variations of circuit parameters.

Based on these considerations, the *output stage* of our basic block can simply consist of an error indication designed to latch and memorize a (00) or (11) due to PSN exceeding the tolerable limits and to do not latch a (00) or (11) due to a tolerable noise. As an example, we here consider to use an error indicator of the kind that we introduced in [17], whose design constraints in relation to circuit parameter variations have been analyzed in [17].

As for the general case of a synchronous system with unencoded outputs, we could connect to the output of each FF a basic block of the kind in Fig. 2, provided that we insert at the input of each block a circuit able to make the NAND receive complementary transitions upon the occurrence of a transition of the FF output. A circuit of this kind can be for instance simply implemented using two transfer gates and an inverter, as shown in Fig. 4.

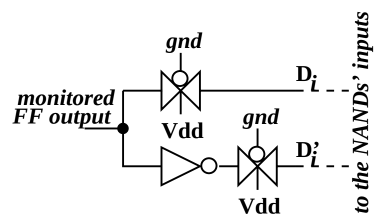

Figure 4. Possible modification of the input stage of our proposed detector to allow its use for synchronous systems with unencoded outputs.

4. VLSI Implementation and Verification

A possible VLSI design of our basic block is shown in Fig. 5, where EI has been designed as in [17].

In particular, we have denoted by RS the external reset signal (and its complement RS') which can be used to start again our system operation after the on-line detection of PSN.

We have implemented our scheme by means of a standard 0.35μm CMOS technology, with a 3.3V power supply (V_{DD}) and (W/L) equal to: i) $(W/L)_n = 1$ and $(W/L)_p = 3$, for the input NANDs; ii) $(W/L)_n = 1$ and $(W/L)_p = 3.7$, for NOT1 and NOT2; iii) $(W/L)_n = 1$ and $(W/L)_p = 5.5$, for NOT3; iv) $(W/L)_p = 8$ and $(W/L)_n = 6.5$, for the feedback inverting gates.

We have verified the described behavior of our basic block by means of electrical level simulations performed using HSPICE.

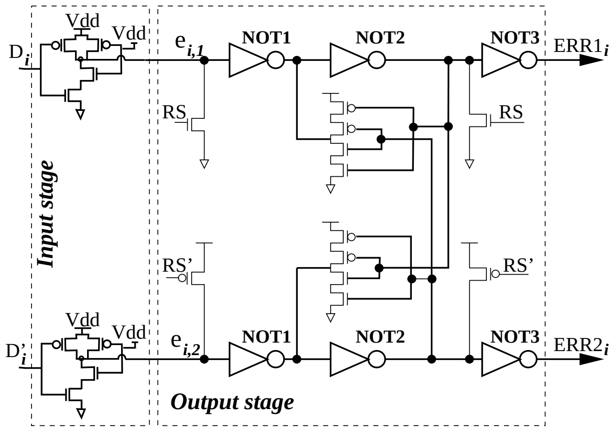

Figure 5. Possible VLSI design of our scheme basic block.

As an example, Fig. 6 shows the waveforms obtained in the case of a transition of the monitored FFs' outputs and no PSN. We can see that our basic cell provides an indication of correct operation ($(ERR1_i, ERR2_i)$ = (10)).

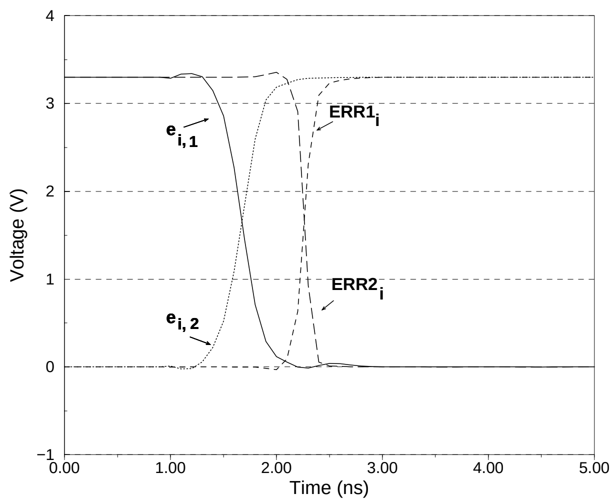

Figure 6. Waveforms obtained in the case of transition of the monitored FFs' outputs (D_i and $D_{i'}$) and no PSN.

Instead, Fig. 7 shows the results obtained in the case of a transition of the monitored FFs' outputs and PSN of $15\% V_{DD}$. We can see that our basic cell provides an output error indication ($(ERR1_i, ERR2_i)$ = (00)).

By means of Monte Carlo simulations, we have also verified that our scheme is able to detect on-line the occurrence of PSN, despite the possible presence of noise affecting also the ground signal and variations of electrical parameters and temperature up to the 10%. Higher parameter variations could also be tolerated by suitably modifying the sensitivity of our scheme (therefore its electrical level design).

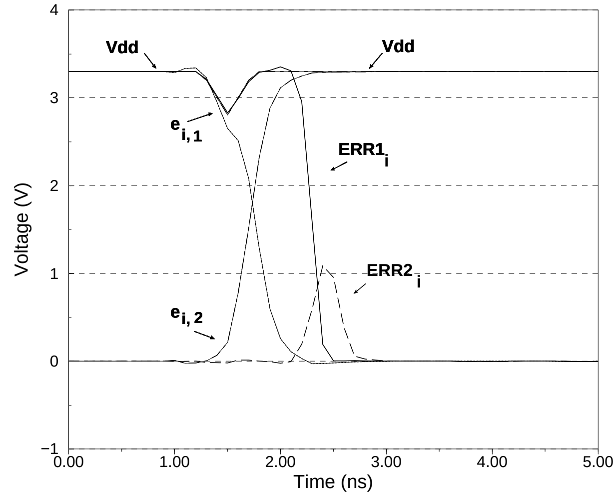

Figure 7. Results obtained in the case of transition of the FFs' outputs and PSN of 15$\% V_{DD}$.

As previously introduced, our scheme could also be implemented using low cost FPGAs. To this purpose a standard gate implementation should be used for the output stage of our basic block (e.g., that in [16]).

5 Costs

The area occupation (A) of our detector, estimated by means of transistors' count, is given by: $A = 16 \cdot 2N$, where $2N$ is the number of monitored FFs. Should the outputs of our basic blocks be joined together to obtain a global error/non error indication, a two-rail code checker (TRC) could be used and an additional area overhead (A') should be considered, where: $A' = 16(N-1)$, or $8(N-1)$, or $(4N+2)$, depending on whether the TRC is designed as in [9], [10], or [13], respectively.

As for the impact of our scheme on system's performance, it is only due to the increase in the capacitive load of the output flip-flops due to our scheme connection, which can be considered negligible.

6 Self-Checking Ability

We must verify that, with respect to possible internal faults, our basic cells are Totally Self-Checking (TSC) [5] or Strongly code-Disjoint (SCD) [18].

We have considered the possible occurrence of faults belonging to a set ($\mathcal{F}$) composed of all possible: node stuck-ats (SAs), transistor stuck-ons (SONs), transistor stuck-opens (SOPs), resistive bridgings (BFs), with values of connecting resistance in the interval $]0, 6k\Omega]$ [19], transient faults (TFs) and delay faults (DFs). In addition, we have considered general fault hypotheses similar to those typically used for self-checking circuits [9], here recalled for clarity: 1) faults occur one at a time; 2) the time elapsing between the occurrence of two successive faults is long enough to allow the application of all possible input codewords.

By means of logical analyses and electrical level simulations we have verified that both the *input* and *output stages* are SCD with respect to all possible SAs, SONs, BFs, TFs, DFs and SOPs, with the exception of the SOPs possibly affecting the feedback inverting gates of EI. As for these undetectable SOPs, however, we should consider that SOPs have been found less likely to occur than the other listed kinds of faults [20] and that their occurrence probability can be further reduced by properly designing the circuit layout [21].

7. Conclusions

We have proposed a self-checking scheme for the on-line detection of PSN exceeding a tolerance bound to be chosen accordingly to system's constraints. Upon the occurrence of such a noise, our scheme provides an output error message, which can then be exploited in order to recover from the detected noise (thus guaranteeing the system's correct operation), or for diagnosis purposes (e.g., if our detector is applied to test chips).

As far as we are concerned, no on-line testing scheme for PSN has been proposed up to now.

For simplicity, our scheme has been described as operating with a two-rail encoded synchronous system. However, we have verified that it can be used also for general unencoded systems, by means of suitably changing its input stage.

Our scheme negligibly impacts system's performance, features self-checking ability with respect to a wide set of possible internal faults and keeps on revealing on-line the occurrence of PSN, despite the possible presence of noise affecting also ground.

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